Specification for CRPS Gen.4 Switching Power Supply AFO

CRPS550NZH-P7LA

Revision:A1.1

Wattage: 550W

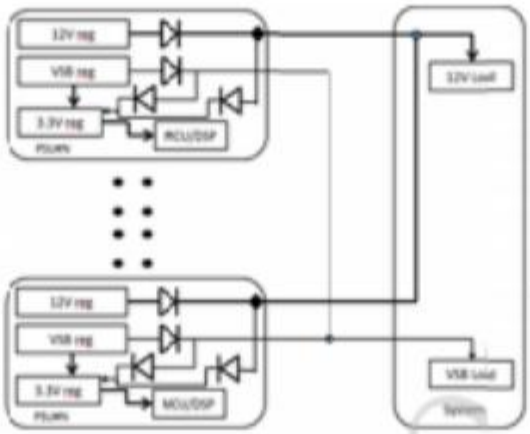
Table of Contents

1 Revision Log

Revision	Description	Approved	Date
A1.0	Initial Release	JZ Shiang	2022/09/20
A1.1	1. Changed D5h FW_REVISION to D2h FW_REVISION 2. 8Eh, changed Primary Hot Spot to Secondary Hot Spot 8Fh, changed Secondary Hot Spot to Primary Hot Spot Added ISP command D5h-D9h 3. Changed the product label, including upgrading the FW version and deleting the side label	JZ Shiang	2022/12/19

2 Scope

This specification establishes the requirements for a custom "1U" form factor, 550W output, active power factor corrected, and wide-range power supply. Also, the approximate dimensions are 73.5mm (W) x 185mm (D) x 40mm (H). The power supply will be used in N+1 redundant operating (N=3) and must contain appropriate Oring devices on all outputs. The number of PSU would be limited to 4.



The below table define the information for both power rating PSU.

API PN	Power Rating	Air flow direction	MKT PN	Customer PN
FSL007-7LAG	550W	AFO		

Power Supply Key Parameter Overview

Application	Sever System	
AC Input & DC input	100-240V_{AC} & 240 V_{DC}	
Power Factor Correction	Active	
Output Power (W)	550W	
Outputs	12V Main Output ($12V_{OUT}$)	Standby (V_{SB})
Nominal Output Voltage	12.00V	12.00 V
Voltage Regulation	± 5%	± 5%
Static load Voltage Regulation	+3%/-4%	± 5%
Minimum Operating Current (A)	0	0
Maximum Operating Current (A)	Output Power / 12.0 V As table. 10	3.0

Table. 1

3.1 Input Conditions

AC input Parameter	Minimum	Nominal	Maximum	Unit
Low Line V_{IN}	90	100-127	132	$V_{AC, RMS}$
High Line V_{IN}	180	200-240	264	$V_{AC, RMS}$
Frequency f_{AC}	47	50/60	63	Hz
V_{BROWN_IN}	80	84	88	$V_{AC, RMS}$
V_{BROWN_OUT}	70	74	79	$V_{AC, RMS}$
V_{IN_OVP}	301		318	$V_{AC, RMS}$
DC input Parameter				
V_{IN}	180	240	320	V_{DC}
V_{BROWN_IN}	167		175	V_{DC}
V_{BROWN_OUT}	155		165	V_{DC}
V_{IN_OVP}	330			V_{DC}

Input Parameter (Max)	550 W
I_{IN} – High Line nominal (AC)	3.6
I_{IN} – Low Line nominal (AC)	7.0
I_{IN} – nominal voltage (DC)	3.6

Table. 2

Note *1: The standby output may continue to operate when input voltage below Vbrown_out range.*

2: Brown-in/Brown-Out can be used 100% ofrated load only above 1V/S variation ofinput voltage, otherwise should become 80% ofrated load forlow slope of Vin.

3. The Iin is specified when the Vin at nominal condition.

4. The AC voltage considering CF= 1.1, 1.6 should meet the turn on/offpoint as above. Due to many waveforms have same C.F result, so the all C.F setting in this specification is based on Chroma instrument setting.

5. Either ofLine or Neutral could be the positive polarity of240Vdc application.

6. The power supply shall not be damaged when the input voltage is in the range of265VAC~300VAC for a long time.

3.2 Input Fuse

A fast-blow and high-breaking-capacity fuse must be placed in the single line fuse on the line/hot wire of the AC input. AC inrush does not cause the ac line fuse to blow under any condition. All protection circuits in the power supply do not cause the ac fuse to blow unless a component in the power supply has failed. The fuse in PSU should be open prior to breaker C32 (e.g. Schneider iC65 series, ABB S260 series, ABB S201 C32A, ABB S202M C32) once internal fail happen.

3.3 Harmonic Current and Power Factor Correction

The power supply shall incorporate universal power input with active power factor corrections, which shall reduce line harmonics in accordance with the EN61000-3-2 and JEIDA MITI standards.

The power factor lists as below:

Load	10%	20%	50%	100%
$P.F._{MIN}$	0.85	0.95	0.98	0.99

Table. 3

Tested at 230Vac, 50/60Hz, measurement environmentshall comply with 80+ or energy star regulation and take the worst result from one of both.

3.4 Input Connector

The AC input receptacleshall be an IEC-320 type C14 capable of at least 15A at $120V_{AC}$ rating and 10A at $250V_{AC}$ rating. This connector is located at the frond side of power supply. There is a retainer to fix the line cord to avoid accident disconnection.

3.5 AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, power supply vendor must provide Intel with written confirmation of dielectric withstand test which includes: voltage level, duration of test and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the $3000V_{AC}$ ($4242V_{DC}$) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements .

3.6 AC Line Dropout / Hold up time

An AC line dropout is defined to be when the AC input drops to $0V_{AC}$ at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC

Table. 4

3.7 AC Line V_{SB} Hold-up time

The V_{SB} output voltage should stay in regulation under its full load (static or dynamic) during an AC line dropout of 70 mS min (= V_{SB} holdup time) whether the power supply is in ON or OFF state (PSON# asserted or de-asserted).

3.8 Auto restart

Auto restart conditions are tested from –40% to –100% AC under voltage conditions for time intervals (T1) ranging from 25 mS to 2 Sec (Max. Load) and 4 Sec (Min. Load) as below matrix table. For each time interval, all of the under voltage conditions listed will be tested. These tests are performed at both the lowest and highest nominal operating AC voltages of the power supply, the output loads settings shall consider Max. and Min. loaded conditions, the available AC duration (T2) on each drop cycle shall be greater than $T_{AC\_ON\_DELAY}$ as specified in section 6.15.

T2

Max. or Min. Load		25ms	40ms	60ms	90ms	130ms	200ms	280ms	400ms	600ms	900ms	1.3S	1.65S	2S	2.4S	2.9S	3.1S	3.45S	4S
Lowest or Highest Nominal Load condition	-40%																		
	-50%																		
	-60%																		
	-70%																		
	-80%																		
	-90%																		
	-100%																		

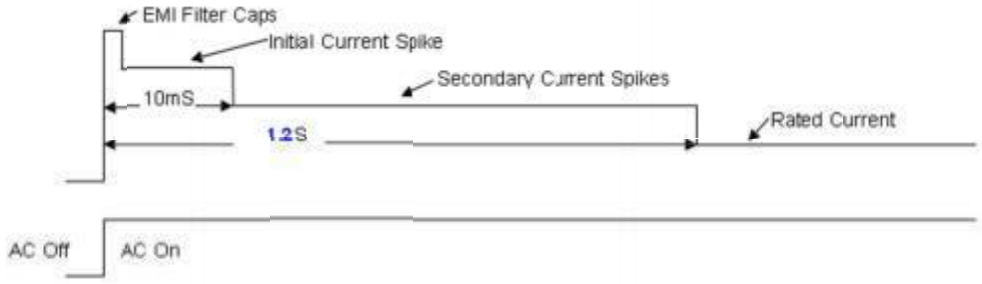
Table. 5

The additional test condition for specific application, the PSU shall be designed to satisfy below requirement, the PSU shall work normally after each condition and meet the turn-on and off sequence during entire validation with all condition specified in this specification, for the condition that is less than $T_{AC\_ON\_DELAY}$ as specified in timing section, the PSU may not be able to turned on but PSU shall resume the normal status once the validation is finish

Cycle	Duty of Input ON	Period (Sec)
10	50%	0.5
		1
		2
		4
		8
		16
		32

3.9 Inrush Current

The power supply shall provide circuitry to limit the turn-on inrush current on any initial current surge or spike of 10ms or less will not exceed limited value in below table, which called as first inrush current. Any additional inrush current surges or spikes in the form of AC cycles or multiple AC cycles greater than 10 mS, and less than 1200 mS, must not exceed value in below table, which called as second inrush current After 1.2 Sec the AC input current must meet the requirements in section 3.1 & 8.1. During a single cycle AC dropout condition or during repetitive ON/OFF cycling of AC, the warm start inrush current must be less than 55A @ 25℃/240V.



Duration (mS)	Wattage	550	Unit
1 – 1200 Cold Start	Inrush current @ 240Vac	15	A_peak
	Inrush current @ 240Vdc	10	

Notes:

1. *The inrush current due to the EMI filter capacitors can be ignored.*
2. *All internal components in the inrush current path. (Included the fuse, bypass diode, currentshunt, bulk rectifiers and surge limiting device) must be able to withstand the surge current without damage the power supply.*
3. *The inrush limiting circuitry shall be designed such that if the active bypass circuitry is noot functional the remaining circuitry shall not cause any smoke/flame potential safety issue.*
4. *The inrush current must meet at cold/ warm start.*
5. *For the timeless than line drop output, the inrush current may exceed than specified value, but the I^2T of input current at this condition shall be less than I^2T of first inrush ccurrent*
6. *For the reppetitive ON/OFF inrush current performance, the minimize period is 10 sec, the AC available duty is 50% of 10sec.*

3.10 Efficiency

The Power supply shall meet 80plus Platinum efficiency requirement at $230V_{AC}$, the measurement and validationshall complete follow 80 plus regulation. In addition, the efficiency performance in 240 Vdc applicationshall be better at least 0.1% than $230V_{AC}$

Loading	20% of max Load	50% of max Load	100% of max Load	Input
Efficiency MIN	90%	94%	91%	230Vac
Efficiency MIN	90.1%	94.1%	91.1%	240Vdc

Table. 6

Note:

1. *Fan loading is not included for efficiency measurements. Efficiency to be measured at 20-25°C after supply has run for 30 minutes.*
2. *The power supply shall pass all efficiency measurements with +0.2% to guarantee design margins forproduction.*

3.11 Line Disturbance

The following requirements for "Line Disturbances" should be over the specified load, temperature of the power supply unless specified otherwise.

Item	Sag	Input Voltage	Input Frequency	Performance Criteria
0 - 1/2 cycle[1]	95%	Nominal AC Voltage Ranges	50 / 60 Hz	No loss of function or performance[2]
> 1 AC cycle	> 30%	Nominal AC voltage Ranges	50 / 60 Hz	Loss of function acceptable, self-recoverable .[3&4]

Item	Surge	Input Voltage	Input Frequency	Performance Criteria
Continuous	10%	Nominal AC voltage Ranges	50 / 60Hz	No loss of function or performance
0 - 1/2 cycle	30%	Nominal AC voltage Ranges	50 / 60Hz	No loss of function or performance

Table. 7

3.12 I_{THD}

This test shall be measured at 230VAC and 50 / 60 Hz

Load	10%	20%	40%	50%
$I_{THD, MAX}$	20%	10%	8%	5%

Table. 8

3.13 Leakage Current

Maximum input leakage current at 264 V_{AC}, 63Hz, shall not exceed 875 uA

[1] *During 0-1/2 cycle test condition as above, the load should be set to as PG holdup time (**T** PWOK_HOLDUP) and minimum load 0A.*

[2] *The power supply may power off under these conditions, it must be capable of restarting, automatically or under program control after the disturbance.*

[3] *The power supply should not be in a latched state such that any ofthe operator buttons/switches do not operate correctly after the disturbance.*

4. When test condition included highline to low line range, Maximum Load should be the rated current ofthe lower voltage range. If the output current larger than rated current ofthe lower voltage range, power supply may latch offdue to output over current protection

3.14 AC Line Transient, Compliable with EMC Standard

Power supply shall operate within specifications under the followings conditions:

IEC 61000-4-2 Electrostatic Discharge – ESD	15kV air discharge, 8kV Contact discharge, Performance Criteria A[1]
IEC 61000-4-3 Radio-Frequency Electromagnetic Field Susceptibility Test – RS	80 ~1000 MHz, 10V/m, Performance Criteria A
IEC 61000-4-4 Electrical Fast Transients /Burst - EFTs	AC Power Port: 1kV / 2kV Performance Criteria A (for 1kV) , Criteria B (For 2kV)
IEC 61000-4-5 Surge Immunity Test:	Per EN55024: 1998/A1: 2001/A2:2003, EN 61000-4-5: Ed. 1.1:2001-04 AC Power Port ~ line to line: 2kV/(2ohm), line to earth (ground): 2kV/(2ohm) Performance Criteria A, Applied stress over than specified but less than 6kV for Line to Line or Line to GND shall not get fire.
IEC 61000-4-6 Conducted Radio Frequency Disturbances Test –CS	AC Power Port; DC Power Port; Signal Ports and Telecommunication Ports: 0.15 ~ 80 MHz, 10Vrms, Performance Criteria A
IEC 61000-4-8 Power frequency magnetic field immunity test	50 Hz or 60 Hz, 1A/m Performance Criteria A
IEC 61000-4-11 Voltage Dips	i) >95% reduction for 0.5 period, ii) 30% reduction for 25 period, iii) >95% reduction for 250 period Performance Criteria B

Table. 9

Note:

Criteria A, The apparatus shall continue to operate as intended. No degradation ofperformance.

Criteria B, The apparatus shall continue to operate as intended, no degradation ofperformance beyond spec limits after test.

Criteria C, Temporary loss offunction is allowed provided the function is self-recoverable or can be restored by the operation ofthe controls.

3.15 EMI

The power supply shall comply with FCC and EN55032 (CISPR22) Class A for conducted and radiated emissions. It must comply at 100 - 120, 200 - 240VAC / 50Hz with 6dB margin as minimum .

3.16 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

4 DC Output Requirements

4.1 Output Load and Status Regulation

The following table provides a summary of specifications for each individual output. The Output voltage must meet the following table under section 3.1, section 4.1 & section 8.1 condition.

Parameter	O/P Wattage (W)	Max Current Rating (A)	Peak Current		Voltage Regulation
			20 Sec	10 mS	
12V main (90-140V_{AC})	550	45	Rated + 6	Rated + 16	Static: +3%/-4% Dynamic: +5%/-5%
12V main (180-264V_{AC})	550	45			
$12V_{SB}$[1]	36	3.0	3.5	--	12.00 V +/-5%

Table. 10

Notes:

1) Length of time peak power can be supported is based on thermal sensor and assertion ofthe SMBAlert# signal. Minimum peak power duration shall be 20 Seconds without asserting the SMBAlert# signal. The peak load requirement should apply to full operating temperature range..

2) The setting of I_{Peak} < I_{OCW} < I_{OCP} needs to be followed to make the CLST work reasonably.

3) Power supply must protect itself in case system doesn't take any action to reduce load based on SMBAlert## signal asserting.

4) The power supply shall support 10 mS peak power at 20% duty cycle step loading for an average current at the current rating.

5) After Peak Current condition, load current should dwell @ full load condition about 10 Minutes before the next Peak current occurred.

6) C14 Inlet current de-rating may exceed during low line Peak Current condition.

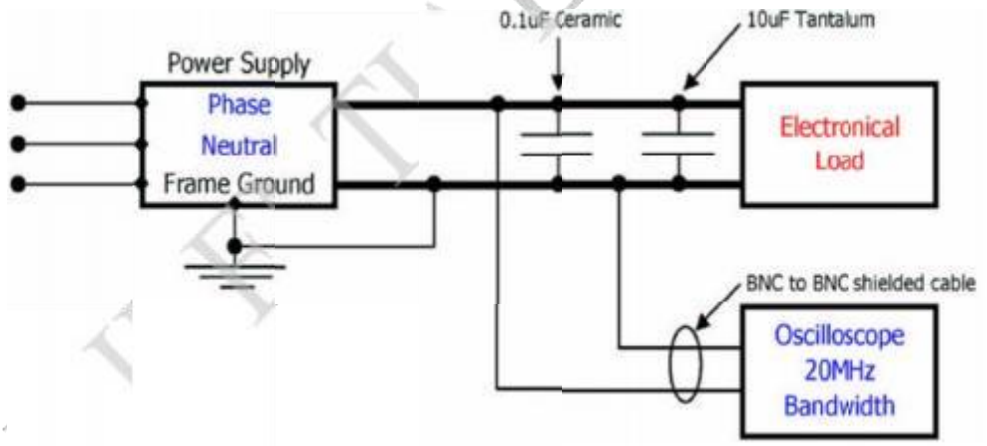
4.2 Standby Output

The V_{SB} output shall be present when an AC input greater than the power supply turn on voltage is applied. There should be load sharing in the standby rail.

4.3 Ripple /Noise

The following output ripple/noise requirements will be met throughout the load ranges specified in section 4.1 and under all input voltage conditions specified in section 3.1 and temperature condition specified in section 8.1 and measured with a resistor load (not an electronic load). Measurement is made with a "SMB to BNC Male Coaxial Cable, 50 Ohm, 1m" connected across the decoupling capacitance and with a 20MHz bandwidth setting in oscilloscope.

Outputs	Maximum	Capacitive Load
12V$_{OUT}$	120 mV $_{PK-PK}$	N.A uF
	105 mV $_{PK-PK}$	270 uF
12VSB	120 mV $_{PK-PK}$	100 uF



Notes:

1. Output ripple & noise should be measured at the pins of the mating output connector, and the Min. load on 12V rail during overall measurement is 1A.
2. Connect the probe with the input tip and ground as short as possible.
3. Output ripple & noise measured with only PS capacitance plus 10 uF ordinary aluminum electrolytic and 0.1uF Ceramic capacitor .
4. Ripple & noise are defined as periodic or random signals over the frequency bannd of 10 Hz to 20 MHz .

4.4 Dynamic Regulation

The output voltageshall remain within the limits specification in section 4.1 Voltage Regulation for the step loading and within the limit specification in below table for the capacitive loading. The load transient repetition rate shall be tested between 50 Hz and 10 kHz at duty cycles ranging from 10%, 50% and 90%.

The Min. output current on 12V rail is 1.0 Ampere.

The load transient repetition rate is only a test specification. The step load may occur anywhere within the Min. load 1A to the Max load show in below table. During $12V_{OUT}$ output load changes from minimum to maximum or maximum to minimum, the power supply must not shutdown.

A special load transient, 100% step load at no load condition, the PSU shall not trigger the any fault and regulation shall at least keep above 11.0V and below 13.4V, this requirement shall be validated in production line 100%.

Outputs[1]	Step Load Size	Slew Rate	Test Capacitor load
$12V_{OUT}$	60%	2.5 A/uS	2200 uF
V_{SB}	1.0A	2.5 A/uS	100 uF

Table. 11

4.5 Audible Noise

No abnormal audible noise is allowed to be generated by the power supply.

4.6 Immune Voltage

The PSU should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500 mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100 mV when AC voltage is applied and the PSON# signal is de-asserted.

4.7 Capacitive Loading

The PSU will be able to power up and operate normally with the capacitive load on the DC outputs (defined by capacitance and ESR), the power supply shall be stable and meet all requirements with the following capacitive loadings.

Outputs	MIN	MAX	Units
V_{SB}	100	3,100	uF
$12V_{OUT}$	2200	22,000	uF

Table. 12

4.8 Turn on/off Overshoot & Undershoot

During the turn-on or turn-off stage, the output voltage including the standby output, under any of the conditions specified in section 4.1 and temperature section 9.1, capacitive loading section 4.6 will less than 10% above the nominal voltage and will settle into the regulation band within 20 mS.

The output voltage undershoot during turn-off of any of the output, including the Standby output, under any of the condition specified in section 4.1 and temperature section 9.1, capacitive loading section 4.5 shall not exceed than 0.3V.

There must be a smooth and continuous ramp of each output voltage from 10% to 95% of its final set point within the regulation band. No voltage of opposite direction will be present on any output during turn- on or turn- off stage, and which shall be measured at 0%/25%/50%/75%/ 100% rated resistive load.

4.9 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

4.10 No Load Condition

This condition shall not trip any failure circuitry shutdown or cause any permanently damaged to the power supply. Also, the power supply shall normal operate when the power supply is turn on or when the power supply is already on at no load condition. Power supply unit shall operate with 0A loading on +12VDC at all specified input voltage condition and any operating environmental requirements.

When the power supply is subsequently loaded, it must begin to regulate and source current without fault.

4.11 Close Loop Stability

The power supply shall be unconditionally stable under all line/load/transient load condition including capacitive load. A minimum of 45 degrees phase margin and 10dB gain margin is required.

The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots.

Bode Plot documentation will have Phase and Gain margin data, line and load conditions, as well as the oscillator injection level. For verification purposes the plots will have the method of test and injection points clearly documented on a current schematic. Stability plots need to be provided at both the upper and lower operating temperature limits.

4.12 Remote ON/OFF

Differential (Single ended) remote sense is to be provided for the designated remote sense outputs. The remote sense must be able to compensate for the defined system output voltage drop over the system output resistance (after the output connector).

The remote sense lines must be protected such that if only the remote sense is connected to the load, or there is a short across the remote sense, the power supply is not damaged.

Note: Make sure the drop compensation is included in determining OV limits.

4.13 Common Mode Noise

The Common Mode Noise on any output shall not exceed 350 mV $_{PK-PK}$ over the frequency band of 10 Hz to 20 MHz.

1. The measurement shall be made across a 100 Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).

2. The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent

4.14 Hot Swap Requirement

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating system. During this process, the output voltageshall remain within the regulation limits specified in section 4.1 with capacitive load specified in section 4.6. The hot swap test must be conducted when the system is operating under static, dynamic condition and zero loading condition.

The power supply should use a latching mechanism to prevent insertion and extraction of the power supply when AC power cord is inserted into the power supply.

4.15 Output Isolation

All power outputs have an isolating device to isolate the power supply from the system power during a power supply failure or during a hot swap operation. This device is located in power supply. This device is an oring diode or functional equivalent.

4.16 Soft Starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

4.17 Force Load Share

The 12V main output will have active load sharing. The output current sharing accuracy refers to section 6.5. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating and does not cause these outputs to go out of regulation in the system.

The power supplies must be able to load share with up to 4 power supplies in parallel and operate in a hot- swap/ redundant N+1 or N+N configurations.

4.18 Load Share Signal Characteristics

The load share signal is only for the load function. The load share signal characteristics can be defined . The delay from output voltages in regulation to load share active with maximum load of one power supply and other power supply in parallel is 100 mS maximum.

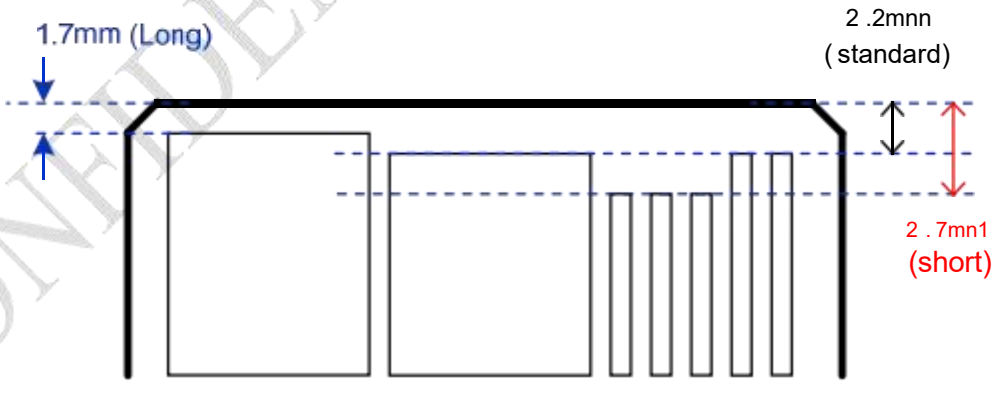
Item	Description	Min	Nominal	Max
V_{SHARE}; I_{OUT}= Max	Voltage of load share bus at specified maximum output current	7.76 V	8.0 V	8.24 V
$\triangle V_{SHARE} / \triangle I_{OUT}$; I_{OUT} >1A	Slope of load share bus voltage with changing load		8.00 / I_{MAX} V/A	
I_{SHARE} sink; V_{SHARE} = 4.00V	Amount of current the load share bus output from each power supply sources.			0.5 mA
I_{SHARE} source V_{SHARE} = 4.00V	Amount of current the load share bus output from each power supply sinks.	4 mA		

Table. 13

4.19 DC Connector and Pin Assignment

Pin No.	Pin Name	Pin Type	Pin Length	Description
A1~A9 B1~B9	GND	$12V_{OUT}$ main & V_{SB} Return	Long	$12V_{OUT}$ main & V_{SB} Return
A10~A18 B10~B18	$12V_{OUT}$	$12V_{OUT}$ main output	Standard	$12V_{OUT}$ main output
A19	SDA	I / O	Short	SMBus / PMBus Data
A20	SCL	I / O	Short	SMBus / PMBus Clock
A21	PSON#	Input	Short	Active low; $12V_{OUT}$ main output on/off control
A22	SMBAlert#	Output	Short	Active low; I^2C alert signal (interrupt)
A23	RETURN Sense	Analog Input	Standard	$12V_{OUT}$ main output Remote Sense -
A24	$12V_{OUT}$ Remote Sense	Analog Input	Standard	$12V_{OUT}$ main output remote sense +
A25	PWOK	Output	Standard	Active high; indicate $12V_{OUT}$ main is valid
B19	A0	Input	Standard	PMBus address 0
B20	A1	Input	Standard	PMBus address 1
B21	12V Standby V_{SB}	Aux Power	Standard	Standby voltage
B22	Smart Redundant Bus	I / O	Standard	Cold Redundancy Bus
B23	$12V_{OUT}$ Load Share Bus	Analog Output	Standard	$12V_{OUT}$ main output load current sharing
B24	Present	Input	Short	Power Supply Present
B25	VIN_GOOD	Output	Short	Indicate the status of input voltage

Table. 14



4.20 Handle Retention

The power supply shall have a handle to assist extraction. The module shall be able to be inserted and extracted without the assistance of tools. The power supply shall have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handleshall protect the operator from any burn hazard and be designed plastic handle or equivalent material.

4.21 Rubber Color

The rubber color at latch mechanism presents the airflow direction of PSU.

Panton 7452C / Blue [DC->AC]: Airflow direction is intake from dc connector and exhausted from the ac connector side of power supply.

4.22 LED Identification

The power supply shall use a bi-color LED; Amber [: 607-613 nm]& Green [: 562-568 nm]. Both LEDs brightness meets the following requirements: Amber 4-12cd/m2, Green 4-12 cd/m2.

4.23 Enhancement performance for input and output transient

In order to assure the PSUs could operate in any input, output or input and output transient normally, the PSU shall be able to prove itself through below enhancement validations.

Redundant Mode (1+1), PSUs shall be able to recovery every single time and all electrical performance is within specification as well as the PMBus status shall only report Input UV, the manufactureshall conduct this performance in ORT stage.

Validation.1, Vin = 220Vrms and AC off time is fixed 3 S, variant parameters are (1) AC ON Time = 3.5 S and 5.0S, both Input AC voltages shall be interleaved turn-on (2) Output Load = 10%, 50% and 100%. (3) Input AC Freq. = 47Hz and 63Hz,total combination condition = 12 sets.

Validation.2, Vin= 220 Vrms / 50 Hz and output dynamic load is set 0-100% with slope rate =2.5 A/uS variant parameters are (1) Frequency of dynamic load = 50/500/5k/10k Hz. (2) duty of dynamic load = 10/50/90% duty, total combination condition = 12 sets.

Validation. 3, Combine previous condition 1 & 2, total combination condition = 24 sets.

Validation. 4, in= 220 Vrms / 50 Hz and output dynamic load is set 0-100% load manually.

5 Protection Requirements

5.1 Primary Protection

The supply must have internal primary over current protection. A fast-blow, hiigh-breaking-capacity fuse must be placed in the line side of the input circuit. This fuse is not to be considered replaceable for purposes of determining power supply reliability and life as specified in Section 8.

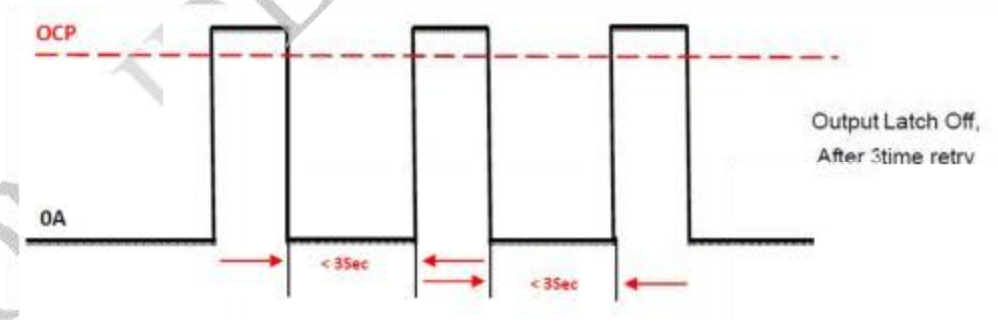
If any component on the line side of the fuse is shorted or opened, it shall not cause a fire or any other safety risk. The power supply must meet the power factor requirements stated in the Energy Star. The boost power factor circuit (PFC) shall protect against bulk capacitor over-voltage due to boost control circuit failure. When a boost over voltage condition is detected, the output +12VDC shall be turned off and the PFC shall be shutdown and operate in latch mode, the booost OV condition set shall prevent any malfunction / false trigger.

5.2 Secondary Protection

The standby power, microprocessor and its I2C communication bus is expected to continue operating under +12VDC fault protection condition. Power to microcontroller circuitry associated with I2C communication shall be from internal standby source AND from user system side source.

5.2.1 Current Limit & Power Protection (OCP & OPP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown, and then retry third time before latchoff. The latch will be cleared only by an AC power interruption. The power supply shall not be damaged from repeated powercycling in this condition.

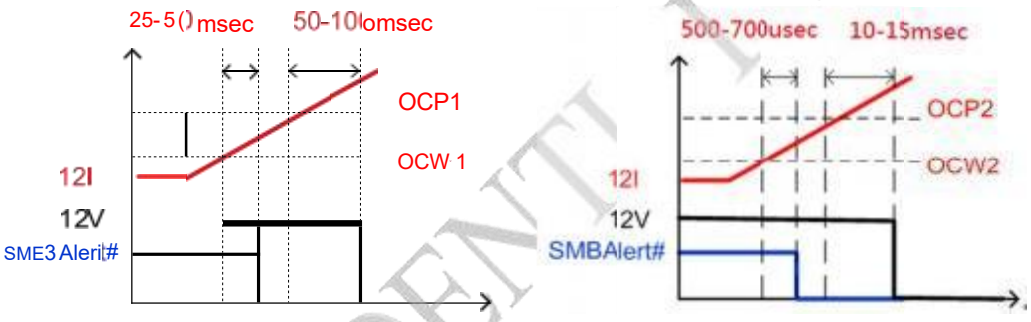


V_{SB} will be auto-recovered after removing OCP limit, the recovery time is 1S with 100ms tolerance.

The SMBAlert and 12V delay time shall be asserted in sequence, the SMBAlert# shall always get asserted at least 80uS before output load (=<170% of rated load)turned off beside the SCP condition.

Spec.	Description	Current Threshold (%)		Trip timing		Testing range	Comments
		MIN	MAX	MIN	MAX		
OCW_1	Slow over current warning (SMBAlert#)	**110**	**120**	**25 mS**	**50 mS**	Rating Load to Max Value of each protection	--
OCP_1	Slow over current protection (shutdown, latch)	**125**	**135**	**50 mS**	**100 mS**		--
OCW_2	Fast over current Warning (SMBAlert#)	**135**	**145**	**500 uSec**	**700 uSec**		Latch and hold for 50-150 mS
OCP_2	Fast over current protection (shutdown, latch)	**145**	**155**	**10mS**	**15 mS**		--
OCP_{SB}	Standby over current protection (shutdown, hiccup mode)	**3.5 A**	**5 A**	**10 mS**	--		10 mS minimum delay

Table. 15



5.2.2 Over and Under Voltage Protection

Outputs	UnderVoltage		OverVoltage		Protection mode	Unit
	Minimum	Maximum	Minimum	Maximum		
V_{SB}	10	11	13.5	14.5	Recovery	V
$12V_{OUT}$	10	11	13.5	14.5	Latch-off	V

Table. 16

Notes:

1. *The above OV/UV test will be satisfied throughout AC input in section 3. 1 and the entire operating temperature*

range in section 9.1

2. A fault on any output other than Standby will not cause the Standby to turn off. Also, that fault on Standby will cause the other outputs to turn off but not latch off.
3. The power supply will provide latch mode except for Standby output.
4. 12V OVP shall re-try three times and then keep latch-off, the interval of retry is 3 Sec, For VSB rail, the time interval is 1 Sec but no latch-off, the VSB shall keep retry until fault removed. The tolerance on time is 100 mS here.

5.2.3 Short Circuit Protection

A short circuit is considered to be resistance of 50 mΩ or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.). The power supply shuts down and latches off for short on main outputs but recovers upon PS_ON toggled or AC re-applied.

5.2.4 Reset after Shutdown

If the power supply latches into a shutdown state due to a fault condition on any output, the power supply will return to normal operation only after the fault has been removed and the power supply has been power-cycled. Both methods of resetting the power supply shall be designed into the supply so that the user may choose which method to use.

Reset can be accomplished in one of two ways as below:

a) Removing AC input power for 10 sec or toggling PSON signal shall be able to reset the latch off protection.

b) Cycling the state of PSON# from on to off to on. The minimum cycle time will be 100 mS.

5.2.5 Over Temperature Protection

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically.

The OTP circuit must have built in hysteresis such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip levelshall have a minimum of 5 °C of ambient temperature hysteresis.

	Trigger Point	Tolerance
Over Temp. warning (OTW)	62 °C	3 °C

Over Temp. Protection (OTP)	65 °C	3 °C

Table. 17

Note: *Internal fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMBAlert# insertion.*

6 Signal Requirement

This requirement shall be met throughout the load regulation condition specified in section 4.1, under all input voltage condition specified in section 3.1 and temperature condition specified in section 9.1. The below table is a TTL signals summary, which presents all the pull-high resistance and pull-up location. The ripple voltage for all TTL signals shall be less than 250 mV @ B.W = 20 MHz with a "SMB to BNC Male Coaxial Cable, 50 Ohm, 1m"

Pin No.	Pin Name	Pin Type (I/O/A)	Active	Pull-up location#4	Pull-up Res. Of system (kΩ)	Pull-up Res. Of PSU (kΩ)	Pull-up Vol. (V)
A19	SDA[1&3]	I / O	--	P	--	10	3.3
A20	SCL[1&3]	I / O	--	P	--	10	3.3
A21	PSON#	I	Low	P	--	10	3.3
A22	SMBAlert#[1]	O	Low	P	--	8.2	<5
A25	PWOK[1]	O	High	P	--	1	3.3
B19	A0[1]	I	--	P	--	10	3.3
B20	A1[1]	I	--	P	--	10	3.3
B22	Smart Redundant Bus	I / O	High	P	--	--	--
B23	$12V_{OUT}$ Load Share Bus	A	--	--	--	--	--
B24	Present	Input	Low	P	--	0	GND
B25	Vin_GOOD#	O	High	P	--	1	3.3

Table. 18

Note:

1. *The signals noted with [1] are designed to be compatible of pull-high voltage for both sides (either of system or PSU), the default is shown above table.*
2. *The function of B25 is reserved for Vin_OK or function, which is different to standard CRPS regulation.*
3. *The pull-up voltage of SDA and SCL could be located on system site and the design could accept 3.3V, if both signals is pulled up by PSU, the high level of SDA and SCL is 3.3V.*

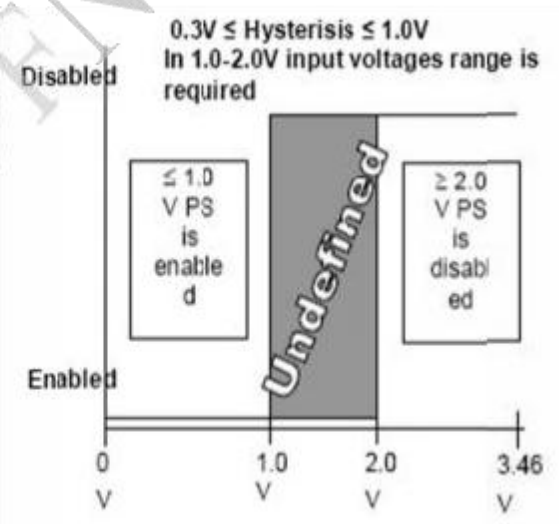
6.1 PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turn on the main power rails. When this signal is not pulled low by the system, or left open, the outputs turn off. The power supply shall provide an internal pull-up resistor to high. The power supply shall also provide de-bounce circuitry on PSON# to prevent it from oscillating On/Off at startup when activated by mechanical switch. Provisions for de-bouncing will be included in the PSON# circuuitry to prevent the power supply from oscillating on/offat startup.

Signal type	Pull-up to internal V_{CC} located in power supply	
PSON# = Low	PSU ON	
PSON# = Open or High	PSU OFF	
	MIN	MAX
Logic level low (PSU ON)	0 V	1 V
Logic level high (PSU OFF)	2.0 V	3.46 V
Source current, $V_{PSON\#}$ = low		4 mA

Table. 19

PSON# signal should be logic level low (PSU ON) when the voltage between 0V ~ 1V, and become logic level high (PSU OFF) when the voltage between 2.0V ~ 3.46V. So the signal may become logic level low when the voltage little larger than 1V, and become logic level high when the voltage little smaller than 2.0V.



6.2 Power Good (PWOK or P_GOOD)

This signal should be asserted high by the power supply to indicate that all outputs are within the regulation thresholds listed in section 4.1. Conversely, this signal should bede-asserted to a low state when any of the DC outputs voltage falls below its under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation can't be guaranteed.

This signal will have an internal pull-up resistor to internal 3.3V sources.

Signal type	Pull-up to VSB located in the power supply.	
PWOK or P_Good = High	DC Outputs O.K.	
PWOK or P_Good = Low	DC Outputs N.G.	
	Minimum	Maximum
Logical Level Low, I_{SINK} = 400 uA	0 V	0.4V
Logical Level High, I_{SOURCE} = 500 uA	2.4V	3.46V
Sink current, PWOK = low		400 uA
Source current, PWOK = high		500 uA
PWOK delay: T_{PWOK_ON}	100 mS	500 mS
Power down delay: T_{PWOK_OFF}	1 mS	
PWOK or P_Good Rise & Fall Time		100 uSec

Table. 20

6.3 PRESENT#

This pin will be tied to Standby return through a resistor. System side should have a pull-up resistor which limits the max current 4mA to go through from this signal pinto the power supply, the pull-down resistorshall be 0 ohm with 1206 package or short PRESENT# to ground directly.

6.4 Load Share Signal

This input / output will allow two or more power supplies to share output current between them. If one of the supplies fails the remaining supplies must pick up the entire load without any of the outputs dropping out of regulation. A defective supply that is connected to the output voltage bus will not have adverse effect on the operation of the remaining function supplies.

Total Load	Number of supplies	V_{LS} (V) Minimum	V_{LS} (V) Nominal	V_{LS} (V) Maximum
100%	2	3.8	4	4.2
50%	2	1.8	2	2.2
20%	2	0.64	0.8	0.96
100%	1	7.76	8	8.24
50%	1	3.8	4	4.2
20%	1	1.4	1.6	1.8
0%	1	0	0	0.3

Table. 21

6.5 Sharing Accuracy

The 12V main will have active load sharing. The failure of a power supply should not affect the load sharing or output voltages of the other supplies, and does not cause these outputs to go out of regulation in the system.

System Load	Sharing Accuracy
100%	± 2%
50%	± 5%
20%	± 10%
10%	± 15%

Table. 22

Note

1: Sharing accuracy is not measured under transient conditions, but under transient conditions a false over current fault must not occur.

2: Current sharing is not required power on of the outputs until the PWOK signal is asserted. (All outputs are valid)

3. The current accuracy shall being getting better with increased load from 10% to 100% of system load.

4. The PSU shall prove the current share performance will be stable during toggle PSON during any load condition in this Specification.

5. The current share performance shall been proved under 3+1 condition and 1+1 condition respectively.

6. The Current share accuracy is calculated by (Deviation current/total current)%, Eg.: total current on system is 20A, and PSU#1 take 8A and PSU#2 take 12A, which accuracy equals (8-10)/(10)%= 20%.

7. The Current share performance shall consider under different Input AC phase as well. E.g: Two PSUs with two different AC sources and the phase between two AC sources shall have 90 phase lag. E.g.2: different AC and DC input configuration on different PSUs in same system.

8. Add 120% ofthe maximum design voltage to the current sharing bus and measure the output voltage variation value. This value shall not exceed the output voltage accuracy range. Recommended: 12V output: 0.25V to 0.4V.

9. Parallel test

A. Under any cross load and input voltage, plug or unplug any power supply, and the overshoot (including undershoot) on the output DC bus must meet the specifications ofthe document.

B. The dynamic response output voltage meets the requirements ofthe system output voltage regulation accuracy under various extreme conditions.

C. 0%, 25%, 50%, 75%, 100% pure resistance load conditions start, the system output voltage power-on waveform must be smooth.

D. Repeatedly plugging and unplugging the module, the power system must not be plugged and pulled to cause other modules to die.

E. Switching, plugging and unplugging the power supply cannot cause the related power supply output signals to be abnormal.

F. Short circuit one of the outputs (short circuit before ORING), the output voltage of the other redundant power supply cannot exceed the specification range.

G. The PSU shall be verified the parallel behavior in any condition specified in this document. Whatever any input voltage combination and static output load condition, the current share performance and ripple voltage of outputshall be within specified regulation.

H. In any different redundancy configuration (1+1, 2+1, 2+2, 3+1 application), enabling the last one PSU by toggling its PSON or input voltage at any load condition shall not cause any deviation to this specification.

6.6 SMBAlert#

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold such as OCW / OTW / OCP , SMB Alert trigger condition please refer FW Spec in detail. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

Signal type	Pull-up to internal 3.3Vsb located in power supply.	
SMBAlert# = High	OK	
SMBAlert# = low	Power Alert to system	
	Minimum	Maximum
Logical Level Low, I_{SINK} = 4 mA	0 V	0.4 V
Logical Level High, I_{SINK} = 50 uA	2.4 V	3.46 V
Sink current, Alert#=low		4 mA
Sink current, Alert# = high		50 uA
Alert# fall time		10 uSec

Table. 23

6.7 Address_A0 / A1

This signal is defined by end user system for PMBus communication, to allocate address of power supply unit in particular slot location. This signal has an internal resistor to internal 3.3 V located in power supply. The address of power supply unit must be set by user system for PMBUS communication reliability.

Signal type	Pull-up to internal 3.3 V located in power supply	
	Minimum	Maximum
Logical Level Low	0 V	0.8 V
Logical Level High	2.0 V	3.46 V

Table. 24

6.8 PMBus CLOCK_SCL & DATA_SDA

SCL is the SMBus clock input to the supply, SDA is the bi-directional SMBus data path to /from the supply. Both signals have a pull-up resistor to 3.3 V internal located in power supply. The pull-up must be diode isolated to prevent an unpowered/ faulted supply from loading the signal. It must be designed to not glitch bus during hot plug and unplugging. The PMBus operation frequency is 100 kHz. It shall conform to SMBus V2.0 signaling protocol standards. And this specification is based on the PMBus specification parts I and II, revision 1.2. The hardware setting in SDA and SCL is

Inner Pulled up Resistor to internal 3.3V = 10k ohm / 0603.

Inner Filter MAX capacitor less than 68pF.

Inner serial Resistor (Rs) = 10 ohm / 0603.

Note:

1. Once the internal communication between primary and second DSP/MCU fault is detected, the Fan speed shall be run at full speed until the fault is removed.

6.9 REMOTE SENSE + / REMOTE SENSE –

These signals are analog Input / Output $12V_{OUT}$ Main Voltage Sense. Both are analog input / output voltage sense lines to compensate for power path voltage drop. These low level analog signals should be isolated from digital circuit noise. When one or more remote sense lines are opened, regulation measured at the power supply output connector must be maintained within regulation defined, plus or minus an additional 200 mV but no more than 300 mV.

6.10 VIN_GOOD#

This signal is an output to indicate AC power is existence and is within operation range. It should act from high to low level within 4 mS only for Vin drops out to zero and input voltage brown-out events. The 4 mS timing is defined as Vin = 0 to Vin_GOOD signallow level.

Signal type	Pull-up 1kΩ to internal 3.3 V located in power supply	
VIN_GOOD = High	Input voltage is in operating range	
VIN_GOOD = low	Input voltage is out of operating range	
	Minimum	Maximum
Logical Level Low, I_{SINK} = 4 mA	0 V	0.4 V
Logical Level High, I_{SINK} = 50 uA	2.4 V	3.46 V
Sink current, VIN_GOOD #= low		4 mA
Sink current, VIN_GOOD # = high		50 uA
VIN_GOOD # rise and fall time		400 uSec

6.11 Smart Redundant Bus

This signal should be connected together at system board for smart redundant function. Please refer to the PMBus specification for detail.

6.12 Standby Turn-off

Following removal of AC power, the Standby output will remain at its steady state value until such time as it begins to decrease in voltage. The decrease will be monotonic in nature dropping to 0.5 V or less. There will be no other perturbations of this voltage at, or following, removal of AC power.

6.13 Fan Speed Control

The power supply shall incorporate a 40 x 28 mm^2 fan for cooling the power supply when installed in the system. The airflow direction shall be from the card edge connector side to the AC inlet side of the power supply (DC->AC) or opposite direction (AC->DC). The Fan speed control must have close loop algorithm based on both the critical component temperature and the ambient temperature (Inlet temperature). Thus ensure the PSU Fan will always ramp to maximum speed under any condition to protect the power supply from overheating.

These conditions include high ambient temperatures, loading, AC input, and airflow impedance.

Under any steady state operating condition (steady state power output level and steady state inlet air temperature), fan oscillationshall be controlled such that associated sound power level variation falls within roughly 10% mean speed. This condition may be treated as steady state fan speed condition. After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60 Sec.

6.14 LED indicators

The power supply may have a single Bi-color (Green-Amber) Configuration, the below table shows the behavior of LED states

Power Supply Condition	LED State
12V Output is normal	GREEN
No AC power to all power supplies	OFF
AC present/Only V_{SB} on (PSoff) or PS in Smart redundant state	1 Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current and slow FAN.	1 Hz Blink AMBER
Power supply critical event causing a shutdown; failure, OCP, SCP, OVP, Fan Fail and OTP	AMBER

Power supply FW updating	2 Hz Blink GREEN

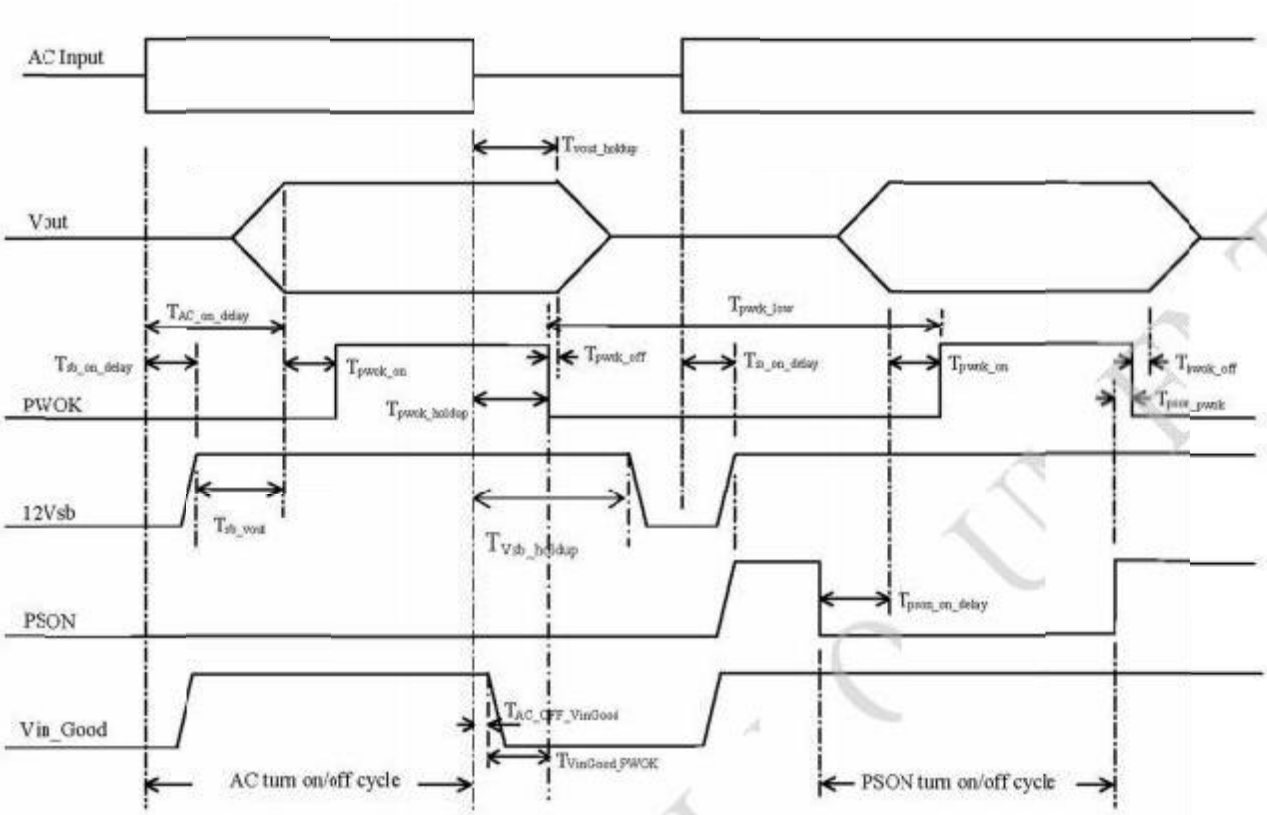
Table. 25

6.15 Timing

These are the timing requirements for the power supply operation. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON# held low and the PSON# signal, with the AC input applied.

ITEM	DESCRIPT ION	MIN	MAX	UNITS
T_{VSB_RISE}	Standby voltage rise time for V_{SB}	1	25	mS
T_{12VOUT_RISE}	Output voltage rise time for $12V_{OUT}$	10	70	
$T_{VSB\_ON\_DELAY}$	Delay from AC being applied to $12V_{SB}$ being within regulation.	--	1500	
$T_{AC\_ON\_DELAY}$	Delay from AC being applied to $12V_{OUT}$ output voltage being within regulation.	--	3000	
T_{12VOUT_HOLDUP}	Time $12V_{OUT}$ output voltage stays within regulation after loss of AC with specified load on section 3.5.	--	--	
T_{PWOK_HOLDUP}	Delay from loss of AC to de-assertion of PWOK with specified load on section 3.5.	--	--	
$T_{PSON\#\_OFF\_DELAY}$	Delay from PSON# de-asserted to power supply turning off.@ half load	--	5	
$T_{PSON\#\_ON\_DELAY}$	Delay from PSON# active to output voltages within regulation limits.	5	400	
$T_{PSON\#\_PWOK}$	Delay from PSON# deactivate to PWOK being de- asserted.	--	5	
T_{PWOK_ON}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	
T_{PWOK_OFF}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	--	
T_{PWOK_LOW}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON# signal.	100	--	
T_{VSB_12VOUT}	Delay from V_{SB} being in regulation to $12V_{OUT}$ output voltage beingin regulation at AC turn on.	50	1000	
T_{VSB_HOLDUP}	Time the VSB standby voltage stays within regulation after loss of AC.	70	--	
$T_{AC\_OFF\_VINGOOD}$	The time interval betwwen AC Drop to zero to VIN_GOOD signal gets asserted.	--	4	
$T_{VINGOOD\_PWOK}$	VIN_GOOD shall be get asserted 1ms prior to PWOK during ac loss event.	1	--	

Table. 26



7 Additional Requirements

7.1 OTP

The power supply shall incorporate a thermal shutdown feature that turns off all outputs when an over temperature condition occurs, the power supply will not be damaged and will automatically restart when the over temp condition no longer exists. Hysteresis shall be employed to prevent a frequent toggling on and off of the outputs, and the hysteresis of OTP shall be greater than 5 Deg-C at least

The location of the OTP sensor should be on the component(s) most likely to overheat in the event of an abnormal ambient temperature or a blockage of airflow.

In normal operation the OTP cannot activate when the power supply is operated in any of the specified operating conditions of sections 3.1, 4.1, and 9.1.

The OTP must be driven low before or at the same time that PWOK is driven low. PWOK must be low for at least 1mS before the main outputs go out of regulation.

7.2 FAN FAIL

The fan(s) is (are) running or the supply is in Standby mode, if there is a fan fault event, the PSU is off and the PWOK must below for at least 1mS before the main outputs go out of regulation. Fan fault detect circuitshall delay to response about 10~15 seconds of ignore time. The main outputshall auto recovery when fault is removed.

8 PMBus

8.1 PMBus requirement

8.1.1 Accuracy for V_{IN}, I_{IN}, P_{IN}, $12V_{OUT}$, I_{OUT}, P_{OUT}

Required Accuracy

	> 10% Load
P_{IN} / E_{IN}	+/- 3% or +/-5W
V_{IN}	+/- 3%
I_{IN}	+/-3% or +/-0.3A
FAN	+/- 500 rpm
$12V_{OUT}$	+/- 2%
I_{OUT}	+/-3% or +/-1 A
P_{OUT}	+/- 3% or +/- 10W
AMB Temperature	+/- 3°C

Table. 27

Note.1: At nominal input voltage measurement. (110Vac/220Vac/270Vdc), the Max. output may be different between low and high line, the load definition where is taken Max. value.

Note.2: In 240Vdc application, no matter the input polarity is positive or negative, the PSU could operate normally, but Accuracy shall be measured when positive polarity on Neutral. If customer may apply positive polarity on either one, please inform early.

Note.3: For light load reporting requirement, in the normal redundant application, PSU shall report below value to system once the below condition is set, which is not included the PSU that in cold redundant mode and set as slave.

When Lin<0.2A, report 0.2A

When Pin<=10W, report 10W

When Iout<1A, report 1A

When Pout<=7W, report 7W

For system power calculation requirement, the reporting performance shall make sure the Pin>Pout situation,

Note.4: The accuracy of AMB temperature is defined as the temperature around the temperature sensor inside of PSU, thereby this accuracy performance shall measure the closest point on the inlet chassis to internal temperature sensor.

8.1.2 Smart Redundancy

Redundant power supplies in a system shall power ON or OFF depending upon loading state. Power supply ON or OFF (in the Smart Standby state) shall power on quickly to maintain full

redundancy in the system. PSU in Cold Standby state should keep a low consumption Pin < 5W, the measurement procedure and setting shall refer to 80 plus protocol.

8.1.3 Black Box

The BLACK BOX should be able to record all the alarm information of the PSU to assist in the later troubleshooting. Need to include but not limited to:

OCP / OPP

Vout OVP

Vout UVP

Fan Fault

OTP

Vin OVP

Note: The output alarm should include 12V main output alarm.

8.1.4 System on-Line Bootloader

The power supply unit has Bootloader function through PMBUS communication. The 12VDC is disable when the Bootloader function is implemented. Please refer FW spec for detail.

9 Environmental Requirements

9.1 Temperature

9.1.1 Normal Operating Ambient (At Sea Level)

Minimum: - 5 °C

Maximum: + 55 °C (Fan Direction: DC->AC); + 55 °C (Fan Direction: AC-> DC);

Maximum rate of change is 10 °C /hr.

The PSU allows a power de-rating operating once the operating temperature is 5°C over specified temperature and the acceptable output load is 80% of output load.

The thermal performance is designed without any shield on air inlet, system shall offer minimum CFM condition for PSU, if both conditions cannot be implemented, please offer the actually environment for further evaluation.

Note: The PSU shall be able to turn-on when AMB = -15 °C condition, the TTLs signal behavior shall be correct, but the regulation could be extended until 13.0V, when the AMB increase back to -5C, all the function shall be within this specification.

9.1.2 Non-Operating Ambient (At Sea Level)

Minimum: - 40 °C

Maximum: + 85 °C

Maximum rate of change is 20 °C /hr.

9.2 Humidity

9.2.1 Operating

5 to 90% relative humidity. (Non-Condensing)

9.2.2 Non-Operating

Up to 95% relative humidity. (Non-Condensing)

9.3 Altitude

9.3.1 Operating

- 50 to 5,000 meter.

NOTE:

1. The system ambient supports at 950m (3,000feet) altitude.

2. Maximum operating temperature is de-rated 1℃ per 125m above 950m.

9.3.2 Non-Operating

-50 to 50,000 feet (15,240 meters)

9.4 Acoustic (Reference Only before DVT stage)

No abnormal audible noise is allowed to be generated by the PSU. The PSU is designed to fulfill the thermal system and PSU requirements with the lowest possible fan speed, the fan speed shall be smoothly increase with ambient and load. The sound levelshall be within following table.

Load	AMB.(C)	dB
20% Load	25	37.6
	35	37.6
50% Load	25	53.2
	35	53.2
100% Load	25	<70
	35	<70

9.5 Thermal shock (none-operating)

Minimum -40°C to Maximum +70°C, transition time not to exceed 5 minutes. Duration of exposure to temperature extremes will be 20 minutes

9.6 Mechanical Shock and Random Vibration

Test	Test Parameter	
Operating Vibration	Sinusoidal Vibration	• Acceleration: 0.25G zero to peak • Frequency Range: 10-500-10Hz • Axis: X,Y,Z • Sweep Speed: 0.25 oct/min • Duration: 1 Sweep
	Random Vibration	• PSD: 0.008G^2/Hz (total 2.0G) • Frequency Range: 10 to 500Hz • Duration: 1 hour/axis • Axis: X,Y,Z
Non-Operating Vibration	Sinusoidal Vibration	• Acceleration: 0.75G zero to peak • Frequency Range: 10-500-10Hz • Axis: X,Y,Z • Sweep Speed: 0.5 oct/min • Duration: 1 Sweep
	Random Vibration	• PSD: 0.008G^2/Hz (total 2.0G) • Frequency Range: 10 to 500Hz • Duration: 1 hour/axis • Axis: X,Y,Z
Operational Half Sine Shock	• 10G, 11ms, half-sine wave pulse. • Both directions on three mutually perpendicular axes.	
Non-Operational Half Sine Shock	• 40G, 11ms, half-sine wave pulse. • Both directions on three mutually perpendicular axes.	
Non-Operational Square Wave Shock	• 40 G, 166in/sec velocity change. • Both directions on three mutually perpendicular axes.	

10 Reliability

10.1 Reliability

Unless otherwise specified, all section 9.0 analyses will be conducted in accordance with the parametric listed below:

The reliabiility requirements are based on the following product usage/application conditions.

AC Input Voltage Range	Refer to Section 3.1
DC Output Load	100% Maximum of rate output load
Temperature Range	Refer to Section 9.1
Relative Humidity	44% ±10% Non-condensing
Altitude	Sea Level
CMTBF	200K Hours @ 80% Load and 55°C
Minimum Operating Life	5 Years @ 80% Load and 45°C, 230Vac
L10	5 Years @ 100% AMB= 45°C, 230Vac

Table. 28

Note:

1. *The Input voltage for CMTBF and operating Life are 100Vac and 200 Vac.*

10.2 E-Cap. Life

All used electrolytic caps must have a usefully life time which exceeds 43,800 Hours at 80% load and normal input and 45°C power supply ambient temperature.

10.3 Burn-in

100% of all engineer stage units (development units) will be burned-in for 24 hours before shipment. The Burn-In profile will be:

Ambient temperature will be (maximum temp. 5℃) with 5℃ ambient tolerance.

All units subjected to burn-in will be at 90~100% of rated load(s). If loading the individual outputs at 90% exceeds the power supply's output rating the loads can be decreased until the power rating of the supply is not exceeded.

Condition 1, All units subjected to burn-in will be exposed to full load condition for 12 hours under low nominal line condition.

Condition 2, All units subjected to burn-in will be exposed to full load to 30 sec power on and 30 sec power off for 1800 sec under low nominal line condition.

Condition 3, All units subjected to burn-in will be exposed to full load condition for 11.5 hour with ½ hour power on and off.

50% of the units subjected to burn-in will have an AC input of low nominal line condition; 50% of the units will have an AC input of high nominal line condition.

10.4 Component De-rating

The component de-rating is designed to satisfy the latest revision of component design guideline, the document number is ELQZ-505-51. The key component de-rating is shown below:

Device Type	Parameter		Stress Factor
Power Rectifiers	Reverse Voltage	V_R	80%
	Forward Current	I_{Fmax}	80%
	Junction Temp.	T_J	80%
Schottky Diode	Reverse Voltage	V_R	95%
	Forward Current	I_{Fmax}	90%
	Junction Temp.	T_J	80%
FET	Breakdown Voltage (>400V)	V_{DSS}	95%
	Drain Current	I_D	80%
	Junction Temp.	T_J	80%

Device Type	Parameter		Stress Factor
Aluminum Electrolytic	Voltage (Bulk Cap)	Vrms	95%
	Ripple Current	Irated	95%
Solid Electrolytic (Oscon)	Voltage (Others)	Vmax	80%
	Temperature	Tmax	90%
Mag. Device Toroid	Flux density	B	80%
Mag. Device Ferrite	Flux density	B	70%

Table. 29

11 EMC and Safety Requirements

The power supply must comply with all regulatory requirements for its intended geographical market. Depending on the chosen market, regulatory requirements may vary. Although a power supply can be designed for worldwide compliance, there may be cost factors that drive different versions of supplies for different geographically targeted markets. The power supply meets below standard, and the mark.

11.1 Safety Mark and Standards

UL/cUL,TUV, CB, CE, CCC and BSMI.

11.2 EMI Requirement

The power supply meet EMI standard as below, need margin 6dB

EN55032 Class A.

CISPR22 Class A.

FCC Class A.

11.3 Hi-pot

The power supply unit must pass a 2550 V_{DC} Residual Voltage test between primary to chassis ground. All production units must pass a 2550 Vdc Hi-Pot test between primary to chassis ground or follow safety agency requirement. The voltage must be ramped up to 2550 within 2.0S and it must be maintained at that level for a minimum of 1 sec. without failure, arc and breakdown or it must comply with safety requirement.

Test voltage	DC
Specify test voltage of Vdc	2550VDC
Current Sensitivity or Current Trip Setting	100uAdc
Ramp-Up Time	2S
Dwell time	1S
RAMP-HI	OFF
Arc fail	ON
Arc sense	5

11.4 Ground Continuity

All production units must pass a ground continuity test with less than 0.1Ω from the safety ground (third wire) input pinto the power supply chassis. Each unit must be marked to indicate it passed the test.

11.5 Anti-smoke

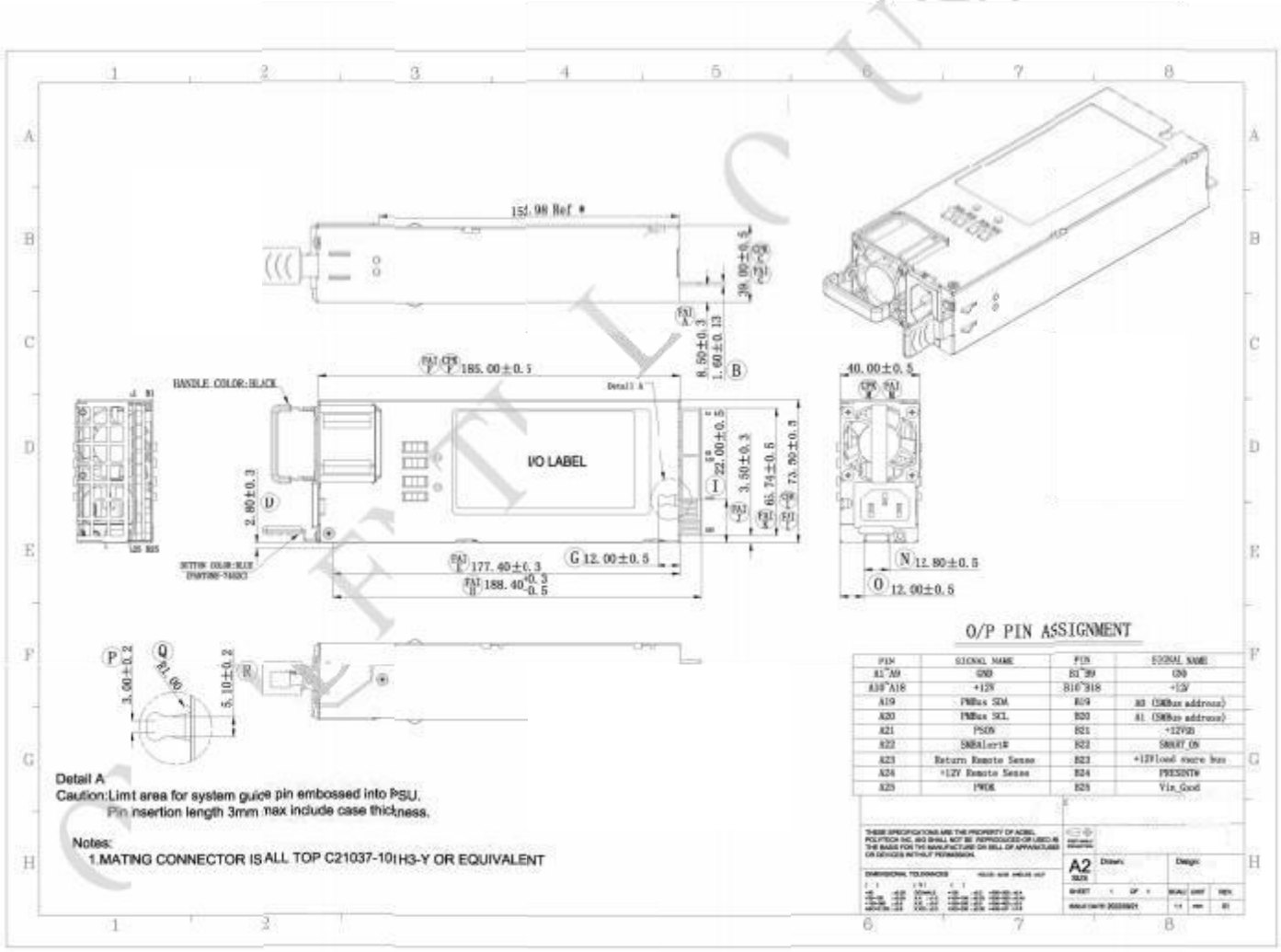
All PSU is designed to meet anti-smoke requirement,
the below situationshall not be happened

- Audible noise during failure of greater than 70 dB (measurement distance 1 m far away AC inlet)
- Visible smoke (aslight smoke could be acceptable, but could not trigger smoke protector)
- Visible spark or fire
- Burning smell

12 Mechanical Drawing

Chassis and cover drawing is shown below. Additional design requirement:

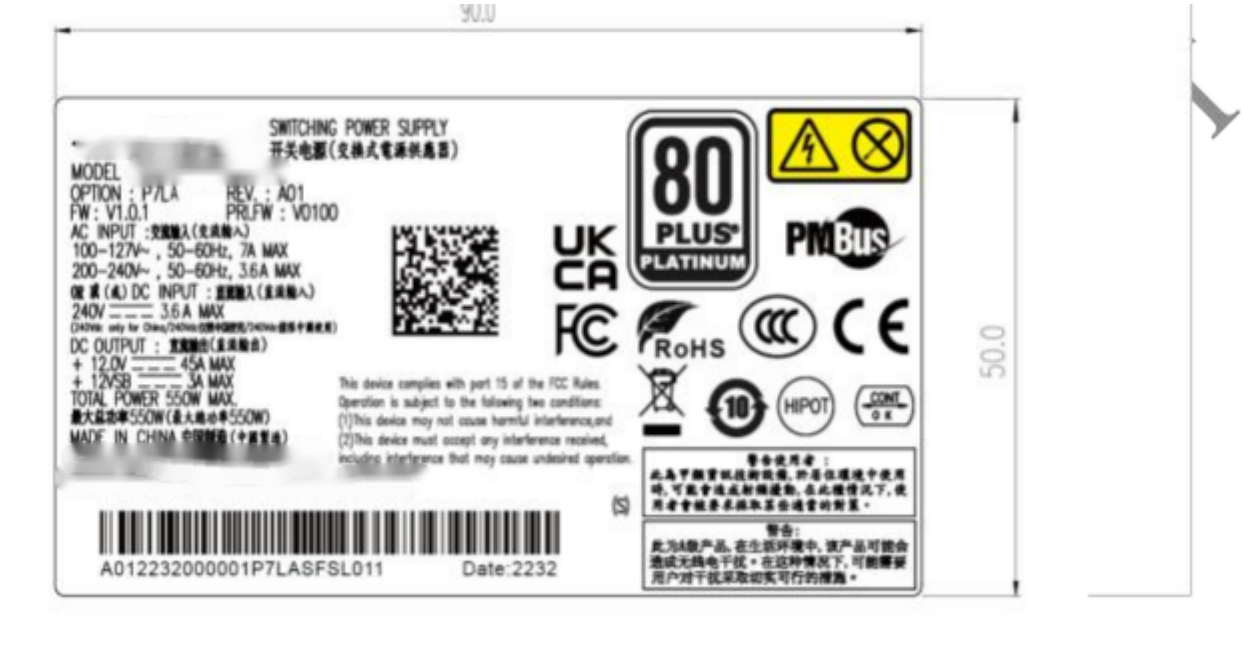
1. Power supply case color: sheet metal primary color (SGCC, no zinc flower)
2. Power handle color: blue PANTONE 7452C
3. Magic Tape color: Black PANTONE
4. Fan shaft front label requirements (given specific requirements: wattage and efficiency)
5. Cable tie: The power cord should have a cable tie to prevent downtime caused by the input line falling off caused by accidental touch on the power cord in the field application.



12.1 Label Drawing (EXAMPLE)

1. Safety label (Below is an example)

Dimension: 90x50mm



12.2 Fan Label

The fan label shall be located on the fan guard to dedicate the Max. output wattage and efficiency level, the fan label dimension is 18 * 18 mm^2 circle, paste on the central of fan guard and align well. The below is an illustration for design reference, both PSUs shall have their own output wattage and efficiency level.

13 Introduction

13.1 FW Scope

This document covers the applicable Power System Monitoring and Management requirements for the HVD C Power Supply with regard to PSU-to-system communications, command and control.

13.2 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2
- System Management Bus (SMBus) Specification Version 2.0

14 General PMBus Requirement

14.1 PSU Address / EEPROM Address

The PSU PMBus device address locations are shown below. For redundant systems there are up to three signals to set the address location of the PSU once it is installed in the system; Address1, Address0. For non-redundant systems the PSU device address location should be B0h. The '0' and '1' correspond to '0' = grounded; '1' = not grounded.

PSU Address	EEPROM Address	Address1	Address0
B0h	A0h	0	0
B2h	A2h	0	1
B4h	A4h	1	0
B6h	A6h	1	1

Table 1: Addressing

14.2 Power Sourcing

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the or'ing device. The PMBus deviceshall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

14.3 Data Speed

The PMBUS device in the power supply shall operate at the full 100 kbps SMBus speed and avoid using clock stretching that can slowdown the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PMBus deviceshall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

Note:

1. Unsupported CMD respond with a NACK, need follow microcontroller datasheet.

14.4 Bus Error

The PMBus deviceshall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10 ms later.

15 PMBus Data Formats

15.1 Bit and Byte Order

When a value consisting of more than one data byte is transmitted, the lowest order byte is sent first and the highest order byte is sent last. Within any byte the MSB is sent first and LSB is sent last.

15.2 Linear Format

15.2.1 Current, input voltage, power, temperature, fan speed, percentage and time

All commands that return a value use linear-11 data format. Only exceptions are output and the READ_EIN/READ_EOUT commands as described in the following sections. The linear data format is a two byte value and contents of mantissa and an exponent.

15.2.2 Output Voltage

All commands that return a value related to output voltage use the linear-16 mode. The exponent for the linear mode can be retrieved from the VOUT_MODE Command. The VOUT_MODE is read-only and has a fixed value.

15.3 Data Formatting Tables

Data range refers to 5.1 PMBus Command List, if a device does support detecting data that is out of the range of the device, itshallset CML error (unsupported data).

READ_IOUT	**N**	
IOUT_OC_FAULT_LIMIT	**Min**	**Max**[1]
IOUT_OC_WARN_LIMIT	**-8**	**N/A-**
MFR_IOUT_MAX		
Note: This formatting applies to all IOUT-related commands.		

Table 2: IOUT Resolution Range

READ_VOUT	**N**	
VOUT_OV_FAULT_LIMIT	**Min**	**Max**
VOUT_UV_FAULT_LIMIT	-9	-9
MFR_VOUT_MIN		
MFR_VOUT_MAX		
Note: This formatting applies to all VOUT-related commands.		

Table 3: VOUT Resolution Range

READ_POUT POUT_OP_FAULT_LIMIT POUT_OP_WARN_LIMIT MFR_POUT_MAX	N	
	Min	Max
	-4	NA
Note: This formatting applies to all POUT-related commands.		

Table 4: POUT Resolution Range

READ_VIN, MFR_VIN_MIN MFR_VIN_MAX	N	
	MIn	Max
	-1	N/A
Note: This formatting applies to all VIN-related commands.		

Table 5: VIN Resolution Range

READ_IIN IIN_OC_FAULT_LIIMIT IIN_OC_WARN_LIMIT MFR_IIN_MAX	N	
	MIn	Max
	-13 or -14	N/A
Note: This formatting applies to all IIN-related commands.		

Table 6: IIN Resolution Range

READ_PIN PIN_OP_WARN_LIMIT MFR_PIN_MAX	N	
	Min	Max
	-7	N/A
Note: This formatting applies to all PIN-related commands.		

Table 7: PIN Resolution Range

READ_FAN_SPEED_n FAN_COMMAND_N(RPM)	N	
	Min	Max
	5	NA

Table 8: FAN SPEED Resolution Range

FAN_COMMAND_N(DUTY)	N	
	Min	Max
	0	NA

Table 9: FAN COMMAND Duty Resolution Range

READ_TEMPERATURE_n	N	
OT_WARN_LIMIT	Min	Max
MFR_TAMBIENT_MAX MFR_MAX_TEMP_n	-1	NA
Note: This formatting applies to all TEMP-related commands.		

Table 10:TEMP Resolution Range

15.4Accuracy（Follow section 8.1)

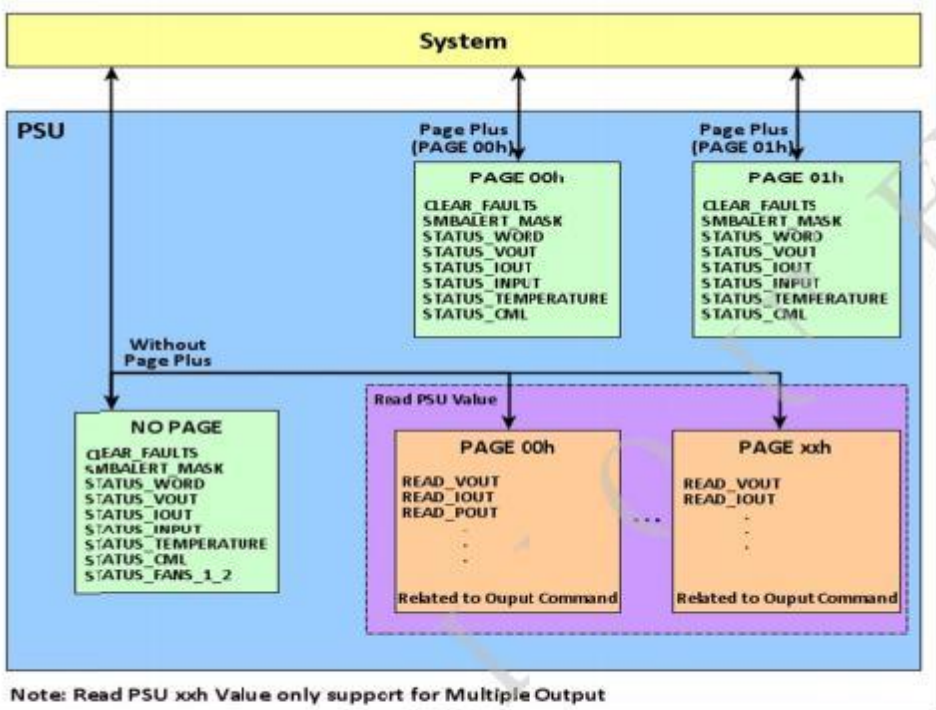
The sensor commands shall meet the following accuracy requirements.

PSU Input Parameter Accuracy as a function of Output Load				
Command	0% ≤load <10%	10% ≤load <20%	20% ≤load <50%	50% ≤load <100%
READ_VIN	Follow section 8.1			
READ_IIN				
READ_PIN				
READ_EIN				
READ_VOUT				
READ_IOUT				
READ_POUT				
READ_EOUT				
READ_TEMPERATURE_n				
READ_FAN_SPEED_n				

Table 11:Accuracy Requirements

16 PMBus Command

System can control and check the PSU in different page information via PAGE_PLUS_CMD or STANDARD_CMD.



16.1 PMBus Command List

All commands have to support PEC and none-PEC.

CMD code	CMD name	SMBus Transaction Type	Data Bytes Length	Format	Value Range	Power On Default Value
01h	OPERATION	R/W Byte	1		n/a	80h
02h	ON_OFF_CONFIG	R/W Byte	1		n/a	1Dh
03h	CLEAR_FAULTS	Send Byte	0		n/a	
05h	PAGE_PLUS_WRITE	Block Write	Variable		n/a	
06h	PAGE_PLUS_READ	Block Write-Block Read Process Call	Variable		n/a	
10h	WRITE_PROTECT	R/W Byte	1		n/a	00h
16h	RESTORE_USER_ALL	Send Byte	0		n/a	
19h	CAPABILITY	Read Byte	1		n/a	B0h

1Ah	QUERY	Block Write-Block Read Process Call	1		n/a	
1Bh	SMBALERT_MASK	Write Word/ Block Write-Block Read Process Call	2		n/a	
20h	VOUT_MODE	Read Byte	1		n/a	17h
21h	VOUT_COMMAND	R/W Word	2		n/a	
3Ah	FAN_CONFIG_1_2	R/W Byte	1		90h or D0h	90h
3Bh	FAN_COMMAND_ 1	R/W Word	2	Linear-11	0 - 100% or 0 - Max rpm	0
40h	VOUT_OV_FAULT_LIMIT	Read Only	2	Linear-16		115% of regulation
41h	VOUT_OV_FAULT_RESPONSE	R/W Byte	1			59H
42h	VOUT_OV_WARN_LIMIT	R/W Word	2	Linear-16	95% ~ 116% of regulation	112.5% of regulation
43h	VOUT_UV_WARN_LIMIT	R/W Word	2	Linear-16	83% ~ 105% of regulation	91.6% of regulation
44h	VOUT_UV_FAULT_LIMIT	Read Only	2	Linear-16		87.5% of regulation
46h	IOUT_OC_FAULT_LIMIT	R/W Word	2	Linear-11	0% ~ 150% max load	130% of max load
47h	IOUT_OC_FAULT_RESPONSE	R/W Byte	1			59h
4Ah	IOUT_OC_ WARN_LIMIT	R/W Word	2	Linear-11	0% ~ 200% of max load	115% of max load
4Fh	OT_FAUL_LIMIT	R/W Word	2	Linear-11	0~512C	65C
50h	OT_FAULT_RESPONSE	R/W Byte	1			C1h
51h	OT_WARN_LIMIT	R/W Word	2	Linear-11	0C ~ 512C	62C
55h	VIN_OV_ FAULT_ LIMIT	Read Word	2	Linear-11	n/a	305V

56h	VIN_OV_ FAULT_ RESPONSE	ReadByte	1		n/a	C1h
57h	VIN_OV_ WARN_LIMIT	Read Word	2	Linear-11	n/a	305V
58h	VIN_UV_ WARN_LIMIT	Read Word	2	Linear-11	n/a	78V
59h	VIN_UV_ FAUL_LIMIT	Read Word	2	Linear-11	n/a	75V
5Ah	VIN_UV_ FAUL_ RESPONSE	ReadByte	1		n/a	C1h
5Bh	IIN_OC_FAULT_LIMIT	Read Word	2	Linear-11	n/a	130% of max load
5Dh	IIN_OC_WARN_LIMIT	Read Word	2	Linear-11	n/a	125% of max load
78h	READ_STATUS_BYTE	Read Byte	1	**bit field**	n/a	
79h	STATUS_WORD	Read Word	2	**bit field**	n/a	
7Ah	STATUS_VOUT	R/W Byte	1	**bit field**	n/a	
7Bh	STATUS_IOUT	R/W Byte	1	**bit field**	n/a	
7Ch	STATUS_INPUT	R/W Byte	1	**bit field**	n/a	
7Dh	STATUS_TEMPERATURE	R/W Byte	1	**bit field**	n/a	
7Eh	STATUS_CML	R/W Byte	1	**bit field**	n/a	
7Fh	STATUS_OTHER	R/W Byte	1	**bit field**	n/a	
80h	STATUS_MFR_SPECIFIC	Read Only	1	**bit field**	n/a	
81h	STATUS_FANS_1_2	R/W Byte	1	**bit field**	n/a	
88h	READ_VIN	Read Word	2	Linear-11		

89h	READ_IIN	Read Word	2	Linear-11		
8Bh	READ_VOUT	Read Word	2	Linear-16		
8Ch	READ_IOUT	Read Word	2	Linear-11		
8Dh	READ_TEMPERATURE_1 (Ambient)	Read Word	2	Linear-11		
8Eh	READ_TEMPERATURE_2 (Secondary Hot Spot)	Read Word	2	Linear-11		
8Fh	READ_TEMPERATURE_3 (Primary Hot Spot)	Read Word	2	Linear-11		
90h	READ_FAN_SPEED_1	Read Word	2	Linear-11		
94h	MFR_READ_FAN_DUTY_CYCLE	Read Word	2	Linear-11	n/a	
96h	READ_POUT	Read Word	2	Linear-11		
97h	READ_PIN	Read Word	2	Linear-11		
98h	PMBUS_REVISION	Read Byte	1	hex integer	n/a	22h
99h	MFR_ID	Block Read	20	ASCII	n/a	
9Ah	MFR_MODEL	Block Read	20	ASCII	n/a	“CRPS550NZH”
9Bh	MFR_REVISION	Block Read	20	ASCII	n/a	"A01"
9Ch	MFR_LOCATION	Block Read	20	ASCII	n/a	“SHENZHEN”
9Dh	MFR_DATE	Block Read	20	ASCII	n/a	YYYY/MM/DD
9Eh	MFR_SERIAL	Block Read	24	ASCII	n/a	Available words are 24bytes in according to P.O.
A0h	MFR_VIN_MIN	Read Word	2	Linear-11	n/a	Refer HW Spec
A1h	MFR_VIN_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec
A2h	MFR_IIN_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec
A3h	MFR_PIN_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec
A4h	MFR_VOUT_MIN	Read Word	2	Linear-16	n/a	Refer HW Spec
A5h	MFR_VOUT_MAX	Read Word	2	Linear-16	n/a	Refer HW Spec
A6h	MFR_IOUT_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec
A7h	MFR_POUT_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec

A8h	MFR_TAMBIENT_MAX	Read Word	2	Linear-11	n/a	Refer HW Spec
A9h	MFR_TAMBIENT_MIN	Read Word	2	Linear-11	n/a	Refer HW Spec
BFh	MFR_FACTORY_MODE	Write Word	2		Refer section 17.16	
D0h	COLD_REDUNDANCY_CONFIG	R/W Byte	1			00h
D2h	FW_REVISION	Block R/W	6			V1.0.1
D4h	MFR_FWUPLOAD_COMPATIBILITY	Read Word	2			
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte	1			
D6h	MFR_FWUPLOAD_MODE	Read Byte	1			
D7h	MFR_FWUPLOAD	Block Write	32			
D8h	MFR_FWUPLOAD_STATUS	Read Word	2			
D9h	MFR_FW_REVISION	Block Read	4			
E4h	MFR_PAGE_X	R/W Byte	1		0<=x<=4 Or FFh	FFh
E5h	MFR_POS_TOTAL	Read Custom	4		refer section 18.5	
E6h	MFR_POS_LAST	Read Custom	4		refer section 18.6	
FEh	MFR_CALIBRATION_EXTEND	Block Write	variable		Refer section 17.17	Only Valid for FactoryMode

Table 12: PMBus Command Table

16.2 Bit Filed

No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.

STATUS_CMD procedure	STATUS_CMD PAGE
Directly (not PAGE_PLUS_CMD)	NO PAGE
Via PAGE_PLUS_CMD PAGE 00h	PAGE 00h
Via PAGE_PLUS_CMD PAGE 01h	PAGE 01h
Via PAGE_PLUS_CMD PAGE xxh	NO PAGE, xx: other value

Table 13:STATUS_CMD procedure

16.2.1 STATUS_WORD

79h	STATUS_WORD (low byte)						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	BUSY	Not Implemented	N/A	N/A	N/A		
6	OFF	This bit is asserted if the unit is not providing power to the output.	OFF	Yes, Reflects realtime state of PSU			
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.	Refer to STATUS_VOUT	Refer to STATUS_VOUT			
4	IOUT_OC_FAULT	An output over current fault has	Refer to STATUS_IOUT	Refer to STATUS_IOUT			

		occurred.			
3	VIN_UV_FAULT	An input under voltage fault has occurred.	Refer to STATUS_INPUT	Refer to STATUS_INPUT	
2	TEMPERATURE	A temperature fault or warning has occurred.	Refer to STATUS_TEMPERATURE	Refer to STATUS_TEMPERATURE	
1	CML	A communications, memory or logic fault has occurred	Refer to STATUS_CML	Refer to STATUS_CML	
0	NONE OF THE ABOVE	Not Implemented	N/A	N/A	

Table 14:STATUS_WORD(low byte)

79h	**STATUS_WORD (high byte)**						
Bits	**Name**	**Description**	**PSU state when bit is asserted('1')**	**STATUS bit Auto Recovery**	**SMBALERT_MASK Default**		
					0 = causes assertion of SMBAlert#		
					1 = does not cause assertion of SMBAlert#		
					NO PAGE	**PAGE 00h (BMC)**	**PAGE 01h (ME)**
7	VOUT	An output voltage fault or warning has occurred.	Refer to STATUS_VOUT	No	N/A		
6	IOUT/POUT	An output current or output power fault or warning has occurred	Refer to STATUS_IOUT	Refer to STATUS_IOUT			
5	INPUT	An input voltage, input current, or input power fault or warning has occurred	Refer to STATUS_INPUT	Refer to STATUS_INPUT			
4	MFR _SPECIFIC	Not Implemented	N/A	N/A			

3	POWER_GOOD#	The POWER_GOOD signal, if present, is negated	Reflects real time state of PSU	Yes, reflects real time state of Power_Good#	
2	FANS	A fan or airflow fault or warning has occurred	Refer to STATUS_FANS	Refer to STATUS_FANS	
1	OTHER	Not Implemented	N/A	N/A	
0	UNKNOWN	Not Implemented	N/A	N/A	

Table 15:STATUS_WORD(high byte)

16.2.2 STATUS_VOUT

7Ah	STATUS_VOUT						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	VOUT_OV_FAULT	VOUT_OV_FAULT (Output Overvoltage Fault)	OFF	No	1, 1, 1		
6	VOUT_OV_WARNING	VOUT_OV_WARNING(Output Overvoltage Warning)	ON	Yes	1, 1, 1		
5	VOUT_UV_WARNING	VOUT_UV_WARNING(Output Undervoltage Warning)	ON	Yes	1, 1, 1		
4	VOUT_UV_FAULT	VOUT_UV_FAULT (Output Undervoltage Fault)	OFF	No	1, 1, 1		
3	VOUT_MAX_WARNING	Not Implemented	N/A	N/A	N/A		
2	TON_MAX_FAULT	Not Implemented	N/A	N/A	N/A		
1	TOFF_MAX_WARNING	Not Implemented	N/A	N/A	N/A		
0	VOUT Tracking Error	Not Implemented	N/A	N/A	N/A		

Table 16:STATUS_VOUT

16.2.3 STATUS_IOUT

7Bh	STATUS_IOUT						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	IOUT_OC_FAULT	Failure	OFF	No	1, 1, 1		
6	IOUT_OC_LV_FAULT	Not Implemented	N/A	N/A	N/A		
5	IOUT_OC_WARNING	Predictive failure	ON	YES	1, 1, 0		
4	IOUT_UC_FAULT	Not Implemented	N/A	N/A	N/A		
3	Current Share Fault	Not Implemented	N/A	N/A	N/A		
2	In Power Limiting Mode	Not Implemented	N/A	N/A	N/A		
1	POUT_OP_FAULT	Failure	OFF	No	1, 1, 1		
0	POUT_OP_WARNING	Predictive failure	ON	YES	1, 1, 1		

Table 17:STATUS_IOUT

16.2.4 STATUS_INPUT

7Ch	STATUS_INPUT						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	VIN_OV_FAULT	Input Overvoltage Fault	OFF	YES	1, 1, 1		
6	VIN_OV_WARNING	Not Implemented	N/A	N/A	N/A		
5	VIN_UV_WARNING	Predictive failure	ON	YES	1, 1, 1		
4	VIN_UV_FAULT	Input Under voltage Fault	OFF	YES	1, 1, 0		
3	Unit Off for Low Input	Either the input	OFF	YES	1, 1, 1		

	Voltage	voltage has never exceeded the input turn-on threshold or if the unit did start, the input voltage decreased below the turn-off threshold.			
2	IIN_OC_FAULT	Input Overcurrent Fault	OFF	No	1, 1, 1
1	IIN_OC_WARNING	Predictive failure	ON	No	1, 1, 1
0	PIN_OP_WARNING	Predictive failure	ON	No	1, 1, 1

Table 18:STATUS_INPUT

16.2.5 STATUS_TEMPERATURE

7Dh	STATUS_TEMPURATURE						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	OT_FAULT	Over Temperature Fault	OFF	YES	1, 1, 1		
6	OT_WARNING	Over Temperature Warning	ON	YES	1, 1, 0		
5	UT_WARNING	Not Implemented	N/A	N/A	N/A		
4	UT_FAULT	Not Implemented	N/A	N/A	N/A		
3	Not implemented	Not Implemented	N/A	N/A	N/A		
2	Not implemented	Not Implemented	N/A	N/A	N/A		
1	Not implemented	Not Implemented	N/A	N/A	N/A		
0	Not implemented	Not Implemented	N/A	N/A	N/A		

Table 19:STATUS_TEMPERATURE

16.2.6 STATUS_CML

7Eh	STATUS_CML						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	Invalid/Unsupported Command	Invalid Or Unsupported Command Received	ON	No	1, 1, 1		
6	Invalid/Unsupported Data	Invalid Or Unsupported Data Received	ON	No	1, 1, 1		
5	Packet Error Check Failed	Packet Error Check Failed	ON	No	1, 1, 1		
4	Not implemented	Not Implemented	N/A	N/A	N/A		
3	Not implemented	Not Implemented	N/A	N/A	N/A		
2	Not implemented	Not Implemented	N/A	N/A	N/A		
1	Not implemented	Not Implemented	N/A	N/A	N/A		
0	Not implemented	Not Implemented	N/A	N/A	N/A		

Table 20:STATUS_CML

16.2.7 STATUS_MFR_SPECIFIC(PSU Input Type)

7Eh	STATUS_CML						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)

7	Not implemented	Not Implemented	N/A	N/A	N/A
6	Not implemented	Not Implemented	N/A	N/A	
5	Not implemented	Not Implemented	N/A	N/A	
4	Not implemented	Not Implemented	N/A	N/A	
3	Not implemented	Not Implemented	N/A	N/A	
2	Not implemented	Not Implemented	N/A	N/A	
1	DC INPUT	DC INPUT	ON	YES	
0	AC INPUT	AC INPUT	ON	YES	

Table 21:STATUS_MFR_SPECIFIC(PSU Input Type)

16.2.8 STATUS_FAN_1_2

81h	STATUS_FANS_1_2 (STATUS_FANS_1_2 command is only accessed by the NO PAGE)						
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#		
					NO PAGE	PAGE 00h (BMC)	PAGE 01h (ME)
7	Fan 1 Fault	Fan 1 fault occurred.	OFF	Yes	1, NA, NA		
6	Fan 2 Fault	Not Implemented	N/A	N/A	N/A		
5	Fan 1 Warning	Fan 1 warning occurred.	ON	Yes	1, NA, NA		
4	Fan 2 Warning	Not Implemented	N/A	N/A	N/A		
3	Fan 1 Speed Overridden	Fan 1 overridden occurred	ON	Yes	1, NA, NA		
2	Fan 2 Speed Overridden	Not Implemented	N/A	N/A	N/A		
1	Airflow Fault	Not Implemented	N/A	N/A	N/A		
0	Airflow Warning	Not Implemented	N/A	N/A	N/A		

Table 22:STATUS_FAN_1_2

16.3 Resetting of Status bits

The STATUS_ commands shall be reset only by the below methods. If the event is still present that caused the assertion of the status bit, the bitshall stay assert after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.
- Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'. CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is setto FFh; all STATUS bits in all PAGEs shall be cleared.
- Cycling input power OFF for 1 second or more then ON shall reset all STATUS_ bits to '0'.
- Systems with redundant power supplies where only one of the supplies cycle input power OFF/ON; the power cycled PSU shall reset the STATUS_ bits to '0' only when powered back ON. If the PSU is kept OFF, the STATUS_ bits shall not be reset.
- Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall be reset only on the assertion of PSON#; not the de-assertion.

16.4 SMBAlert_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits.

SMBALERT_MASK procedure	MASK STATUS_CMD PAGE
Directly (not PAGE_PLUS_CMD)	NO PAGE
Via PAGE_PLUS_CMD PAGE 00h	PAGE 00h
Via PAGE_PLUS_CMD PAGE 01h	PAGE 01h
Via PAGE_PLUS_CMD PAGE xxh	NO PAGE, xx: other value

Table 23:SMBALERT_MASK procedure

16.5 SMBAlert#

16.5.1 Alert Response Address (ARA)

The PSU shall not support ARA. After asserting the SMBAlert# signal the PSU shall keep its address at it standard address.

16.5.2 SMBAlert# operation in standby mode

The PSU shall assert the SMBAlert# signal only when the main outputs are ON. SMBAlert# shall stay de-asserted when the PSU is in standby mode when any bits in the STATUS commands get asserted.

16.5.3 Setting and Resetting the SMBAlert# signal

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level deteected event. Whenever the event is present SMBAlert# shall be asserted. The SMBAlert# signal shall not de-aassert at any time if the event that has caused the assertion is still present.

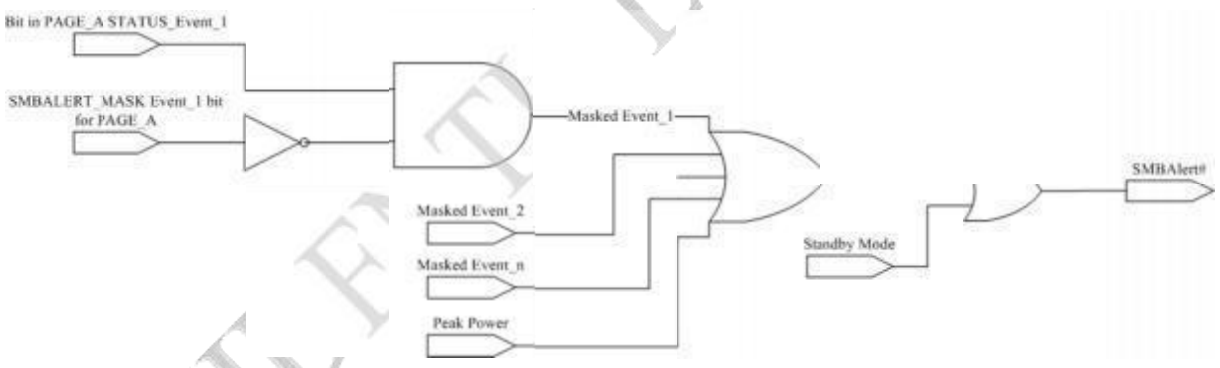
The SMBAlert# signal shall be cleared and re-armed by the following methods.

- Clearing STATUS bits causing the asserted SMBAlert# signal.
- Power cycling with PSON or with input power.
- Masking the event with SMBALERT_MASK.

16.5.4 Continuous Assertion After Clearing If Condition Is Still Present

If the warning or fault condition is present when a bit is cleared, the bit and associated SMABLERT# signal stays asserted with no momentary transition to a de-asserted state.

16.5.5 Conceptual Schematic of SMBAlert#



Note: Peak Power Refer to HW spec

17 PMBus Command Details

17.1 PAGE (00h)

The PAGE command provides the ability to configure, control and monitor different Output through only one physical address.

Each PAGE contains the Operating Memory for eeach output and shall allow system to access corresponding Memory after the PAGE had been switched with the PAGE command.

PAGE	Output	CMD Support
00h	12V(main output)	READ_VOUT, READ_IOUT, READ_POUT …

Table 24:PAGE

Note:

1. PAGE 00h applies to all Main output-related commands.
2. Other PAGE, Read_Value Command configure to PAGE 00h.

17.2OPERATION(01h)

The OPERATION command is used to turn the unit on and off in conjunction with the input from the CONTROL pin.

01h	OPERATION		
Bits	Value	CONTROL pin	Unit on and off
7	0	ON	ON
	0	OFF	OFF
	1	ON	ON
	1	OFF	ON
6:0	Not implemented		

Table 25:OPERATION

17.3ON_OFF_CONFIG(02h)

THE ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off.

02h	ON_OFF_CONFIG		
Bits	Description	Value	Meaning
7:5	Not implemented	X	Reserved
4	Sets the default to either operate any time ower is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin.
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command(as programmed in bits [3:0]).
3	Control how the unit responds to commands received via the	0	Unit ignores the on/off portion of the OPERATION command from serial bus.

	serial bus	1	To start,the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit[2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Control how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin(on/off control only the OPERATION command)
		1	Unit requires the CONTROL pinto be asserted to start the unit. Depending on bit [3],the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Not implemented	X	Not implemented
0	CONTROL pin action when commanding the unit to turnoff	0	Reserved
		1	Turn off the output and stop transferring energy to the output as fast as possible.

Table 26:ON_OFF_CONFIG

17.4CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is able to reset all STATUS bit of instance or all instances simultaneously and this command does not cause a unit that has latched off for a fault condition to Restart. If the fault is still present when the bit is cleared, the fault bitshall immediately be set again and the host notified by the usual means.

The CLEAR_FAULTS command can be issued directly or via PAGE_PLUS_WRITE. Refer CLEAR_CAULTS table.

CLEAR_FAULTS procedure	Reset STATUS registers PAGE
Directly (not PAGE_PLUS_WRITE)	NO PAGE
Via PAGE_PLUS_WRITE PAGE 00h	Only PAGE 00h
Via PAGE_PLUS_WRITE PAGE 01h	Only PAGE 01h
Via PAGE_PLUS_WRITE PAGE FFh	All page(NO PAGE, PAGE 00h, PAGE 01h)

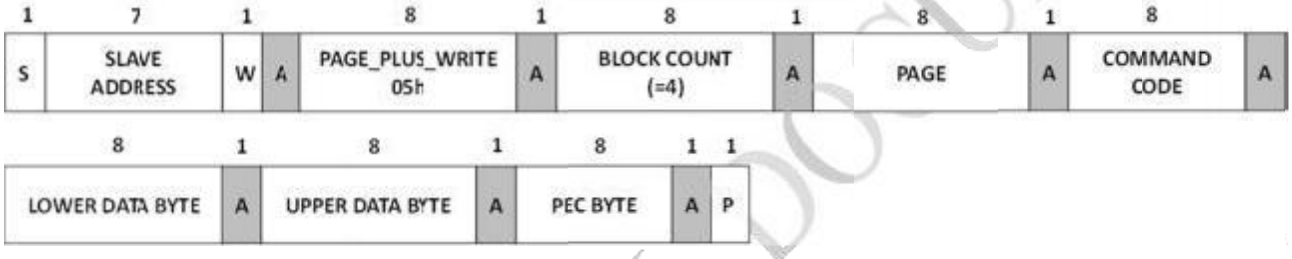
Table 27:CLEAR_FAULTS procedure

17.5 PAGE_PLUS_WRITE / PAGE_PLUS_READ commands (05h/06h)

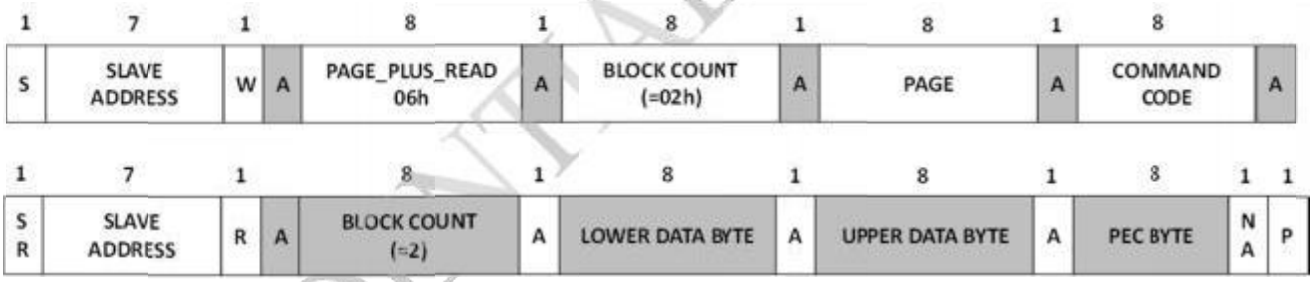
The PAGE_PLUS_WRITE (05h) and PAGE_PLUS_READ (06h) commands, defined in following subsections, are used with the STATUS_BYTE, STATUS_WORD, STATUS_VOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_CML, CLEAR_FAULT and SMBALERT_MASK to create two instances of the same command. Each instance is set by the same events, but cleared by their own master in the system.

All STATUS commands, except the STATUS_FANS_1_2 commands, shall be accessed with the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands. PAGE_PLUS_ commands used with STATUS_FANS_1_2 and STATUS_CML – OTHER commands shall be treated as "unsupported data".

PAGE_PLUS_WRITE Packet Format Example:



PAGE_PLUS_READ Packet Format Example:



Note: PAGE_PLUS commands shall not affect the currently set Page Memory.

17.6 WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device.. The intent of this command is to provide protection against accidental changes.

All supported commands may have their Parameters read, regardless of the WRITE_PROTECT setting s except Cold_Redundancy_Config (D7h), MFR_BLACKBOX_PAGE (E4h) and ISP.

10h	WRITE_PROTECT
Value	Meaning
80h	Disable all writes except to the WRITE_PROTECT command

40h	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands
20h	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE, ON_OF_CONFIG and VOUT_COMMAND commands
00h	Enable writes to all commands (Default value).

Table 28：WRITE_PROTECT

Note: If a device receives a data byte that is not listed, then the device shallset CML error (unsupported data)

17.7 CAPABILITY (19h)

19h	CAPABILITY		
Bits	Description	Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
3:0	Not implemented	X	Reserved

Table 29：CAPABILITY

17.8 QUERY (1Ah)

1Ah	QUERY	
Bits	Value	Meaning
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read

4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data
1:0	XX	Reserved for future use

Table 30:QUERY

17.9 QUERY Value

CMD Code	CMD Name	QUERY Value
00h	PAGE	F0h
01h	OPERATION	FCh
02h	ON_OFF_CONFIG	FCh
03h	CLEAR_FAULTS	DCh
05h	PAGE_PLUS_WRITE	DCh
06h	PAGE_PLUS_READ	BCh
10h	WRITE_PROTECT	FCh
16h	RESTORE_USER_ALL	DCh
19h	CAPABILITY	BCh
1Ah	QUERY	BCh
1Bh	SMBALERT_MASK	FCh
20h	VOUT_MODE	BCh
21h	VOUT_COMMAND	E0h
3Ah	FAN_CONFIG_1_2	FCh
3Bh	FAN_COMMAND_1	E0h
40h	VOUT_OV_FAULT_LIMIT	A0h
41h	VOUT_OV_FAULT_RESPONSE	FCh
42h	VOUT_OV_ WARN _LIMIT	E0h
43h	VOUT_UV_ WARN _LIMIT	E0h

44h	VOUT_UV_ FAULT _LIMIT	A0h
46h	IOUT_OC_FAULT_LIMIT	E0h
47h	IOUT_OC_FAULT_ RESPONSE	FCh
4Ah	IOUT_OC_WARN_LIMIT	E0h
4Fh	OT_ FAULT _LIMIT	E0h
50h	OT _FAULT_ RESPONSE	FCh
51h	OT_WARN_LIMIT	E0h
55h	VIN_OV_FAULT_LIMIT	A0h
56h	VIN_OV_FAULT_RESPONSE	BCh
57h	VIN_OV_ WARN _LIMIT	A0h
58h	VIN_UV_ WARN _LIMIT	A0h
59h	VIN_UV_ FAULT _LIMIT	A0h
5Ah	VIN_UV_ FAULT _ RESPONSE	BCh
5Bh	IIN_OC_FAULT_LIMIT	A0h
5Dh	IIN_OC_WARN_LIMIT	A0h
78h	READ_STATUS_BYTE	BCh
79h	STATUS_WORD	BCh
7Ah	STATUS_VOUT	FCh
7Bh	STATUS_IOUT	FCh
7Ch	STATUS_INPUT	FCh
7Dh	STATUS_TEMPERATURE	FCh
7Eh	STATUS_CML	FCh
7Fh	STATUS_OTHER	FCh
80h	STATUS_MFR_SPECIFIC	BCh
81h	STATUS_FANS_1_2	FCh
88h	READ_VIN	A0h
89h	READ_IIN	A0h
8Bh	READ_VOUT	A0h
8Ch	READ_IOUT	A0h
8Dh	READ_TEMPERATURE_1(Ambient)	A0h
8Eh	READ_TEMPERATURE_2(Secondary Hotspot)	A0h
8Fh	READ_TEMPERATURE_3(Primary Hotspot)	A0h
90h	READ_FAN_SPEED_1	A0h
94h	MFR_READ_FAN_DUTY_CYCLE	A0h
96h	READ_POUT	A0h

97h	READ_PIN	A0h
98h	PMBUS_REVISION	BCh
99h	MFR_ID	BCh
9Ah	MFR_MODEL	BCh
9Bh	MFR_REVISION	BCh
9Ch	MFR_LOCATION	BCh
9Dh	MFR_DATE	BCh
9Eh	MFR_SERIAL	BCh
A0h	MFR_VIN_MIN	A0h
A1h	MFR_VIN_MAX	A0h
A2h	MFR_IIN_MAX	A0h
A3h	MFR_PIN_MAX	A0h
A4h	MFR_VOUT_MIN	A0h
A5h	MFR_VOUT_MAX	A0h
A6h	MFR_IOUT_MAX	A0h
A7h	MFR_POUT_MAX	A0h
A8h	MFR_TAMBIENT_MAX	A0h
A9h	MFR_TAMBIENT_MIN	A0h
D0h	COLD_REDUNDANCY_CONFIG	FCh
D2h	FW_REVISION	BCh
E4h	MFR_PAGE	F0h
E5h	POS_TOTAL	BCh
E6h	POS_LAST	BCh

Table 31：QUERY Value

17.10 VOUT_MODE (20h)

20h	VOUT_MODE	
Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command
VID	001b	Five bit VID code identifier per
Direct	010b	Always set to 00000b

Table 32：VOUT_MODE

17.11 FAN_CONFIG_1_2 (3Ah)

3Ah	FAN_CONFIG_1_2	
Bit	Value	Meaning
7	1	A Fan Is Installed In Position 1
	0	No Fan Is Installed In Position 1
6	1	Fan 1 Is Commanded In RPM
	0	Fan 1 Is Commanded In Duty Cycle
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	1	A Fan Is Installed In Position 2
	0	No Fan Is Installed In Position 2
2	1	Fan 2 Is Commanded In RPM
	0	Fan 2 Is Commanded In Duty Cycle
1:0	00b-11b	Fan 2 Tachometer Pulses Per Revolution

Table 33:FAN_CONFIG_1_2

17.12 MFR_READ_FAN_DUTY_CYCLE (94h)

The MFR_READ_FAN_DUTY_CYCLE command returns the duty of the PMBus device's fan control in percent. This command is read only. The two data bytes are formatted in the Linear Data format.

17.13 FRU Command (0x99~0x9E)

Data1	Data2~Data21	CMD
0x14(20)	Data string with ASCII code, the free bytes fill with 0x20	0x99-x9D
0x18(24)	Data string with ASCII code	0x9E

Table 34:FRU Command

17.14 Warning and Fault Limit

Warning limits shall be set with enough margin to guarantee no false warnings will occur is PSU operates within the specified requirements, but before the PSU shuts down. Fault limits shall be set at limits equal to or greater than the level at which the PSU shuts down.

The PSU shall reset the warning and fault limits to default values for the following case.

- Input power cycling
- PSON power cycling
- High / Low Line change

Note:

1. IIN_OC warning and fault Limit has diffident value in High/Low input.
2. If High/Low line has diffident max load than limits will change with input.

3. Warning and fault limits will not be stored within the non-volatile User Store memory when limit change by command write data.

4. RESTORE_USER_ALL (16h) command can copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory.

17.15 Fault Response

Commands are provided to set the response to each fault condition. These commands have one data byte that describes how the device should respond to the fault. Each of the fault response commands requires that the user make three choices about how the device will respond to the fault condition. The PSU shall reset the fault response to default values for the following case.

- Input power cycling
- PSON power cycling

Note:

1. Fault Response will not be stored within the non-volatile User Store memory when limit change by command write data.
2. RESTORE _USER_ALL (16h) command can copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory

17.15.1 Voltage,Temperature And TON_MAX Faults Response Data Byte

Bits	Description	Value	Meaning
7:6	Response	00	The PMBus device continues operation without interruption.
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).

		10	The deviceshuts down (disables the output) and responds according to theretry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The minimum number is 1 and the maximum number is 6. If the device fails to restart (the fault condition is no longer present and the device is delivering power to the output and operating as programmed) in the allowed number of retries, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shutdown.
2:0	Delay Time	XXX	The number of delay time units, which vary depending on the type of fault. This delay time is used for either the amount of time a unit is to continue operating after a fault is detected or for the amount of time

			between attempts to restart.

Table 35:Voltage, Temperature And TON_MAX Faults Response Data Byte Details

17.15.2 VOUT_OV_FAULT_RESPONSE (41h)

41h	VOUT_OV_FAULT_RESPONSE	
Bit	**Value**	**Description**
7:6	00	Not implemented
	01	Refer Table 35
	10	Refer Table 35
	11	Not implemented
5:3	000	Refer Table 35
	001-110	Refer Table 35
	111	Not implemented
2:0	000-111	Refer Table 35; Configure to attempts reset time, time unit: 3s.

Table 36:VOUT_OV_FAULT_RESPONSE

17.15.3 OT_FAULT_RESPONSE (50h)

50h	OT_FAULT_RESPONSE	
Bit	**Value**	**Description**
7:6	00	Not implemented
	01	Refer Table 35
	10	Refer Table 35
	11	Refer Table 35
5:3	000	Refer Table 35
	001-110	Refer Table 35
	111	Not implemented
2:0	000-111	Refer Table 40; Configure to fault detect time, time unit: 2s.

Table 37:OT_ FAULT_ RESPONSE

17.15.4 VIN_OV_FAULT_RESPONSE (56h)

56h	VIN_OV_FAULT_RESPONSE	
Bit	**Value**	**Description**

7:6	00	Not implemented
	01	Refer Table 35
	10	Refer Table 35
	11	Refer Table 35
5:3	000	Refer Table 35
	001-110	Refer Table 35
	111	Not implemented
2:0	000-111	Refer Table 35; Configure to fault detect time, time unit: 200ms.

Table 38:VIN_OV_FAULT_RESPONSE

17.15.5 VIN_UV_FAULT_RESPONSE (5Ah)

5Ah	VIN_UV_FAULT_RESPONSE	
Bit	**Value**	**Description**
7:6	00	Not implemented
	01	Refer Table 35
	10	Refer Table 35
	11	Refer Table 35
5:3	000	Refer Table 35
	001-110	Refer Table 35
	111	Not implemented
2:0	000-111	Refer Table 35; Configure to fault detect time, time unit: 1s.

Table 39:VIN_UV_FAULT_RESPONS

17.15.6 Current Fault Response Data Byte Details

Bits	Description	Value	Meaning
7:6	Response	00	The PMBus device continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT.

		01	The PMBus device continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT. If the output voltage is pulled down to less than that value, then the PMBus deviceshuts down and responds according to the Retry setting in bits [5:3].
		10	The PMBus device continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0] and the delay time units for specified in the IOUT_OC_FAULT_RESPONSE. If the device is still operating in current limiting at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The PMBus deviceshuts down and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000	A zero value for the R Settin means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The minimum number is 1 and the maximum number is 6. If the device fails to restart (the fault condition is no longer present and the device is delivering power to the output and operating as programmed) in the allowed number of retries, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.

		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shutdown.
2:0	Delay Time	XXX	The number of delay time units, which vary depending on the type of fault. This delay time is used for either the amount of time a unit is to continue operating after a fault is detected or for the amount of time between attempts to restart.

Table 40: Current Fault Response Data Byte Details

17.15.7 IOUT_OC_FAULT_RESPONSE (47h)

47h	IOUT_OC_FAULT_RESPONSE	
Bit	**Value**	**Description**
7:6	00	Not implemented
	01	Refer Table 40
	10	Refer Table 40
	11	Not implemented
5:3	000	Refer Table 40
	001-110	Refer Table 40
	111	Not implemented
2:0	000-111	Refer Table 40; Configure to attempts reset time, time unit: 3s.

Table 41: IOUT_OC_FAULT_RESPONSE

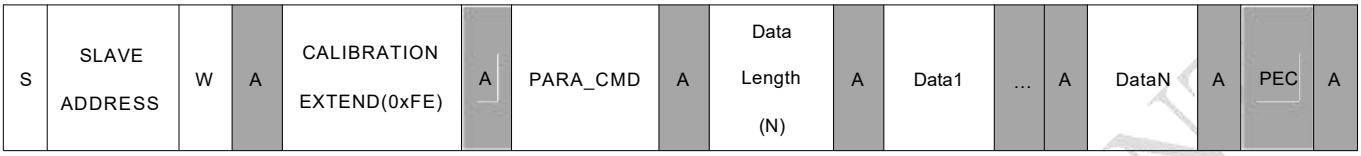
17.16 MFR_FACTORY_MODE (0xBF)

The MFR_FACTORY_MODE (0xBF) command is used to Enable/Disable Factory mode. MFR_CALIBRATION_EXTEND(0xFE) is enabled only when the PSU work in Factory mode.

BFh	MFR_FACTORY_MODE
Value	Meaning
CDABh	Factory Mode is enabled.
others	Factory Mode is disabled. (Default value:0xFFFF)

17.17 MFR_CALIBRATION_EXTEND(0xFE)

The MFR_CALIBRATION_EXTEND (0xFE) command is used to write Production Data or calibrate the parameters of the PSU. The Command is valid only when the PSU work in Factory Mode. It's a Block Write command. The command format is:



FEh	MFR_CALIBRATION_EXTEND		
PARA CMD	Description	Data Length	Data
0x00	Write SN of the PSU	20	Ascii,"3312345678901234"
0x01	Write DATE of the PSU	20	Ascii,"2021/01/21"
0x11	Calibrate 12VLS Reference	2	0-4700
0x12	Save Calibration Data	2	0xAB 0xCD
0x14	Calibrate 12VLS Display Value	2	ActualValue*512 12V:00 18
0x16	Calibrate 12V Voltage Reference	2	ActualValue*512 12V:00 18
0x17	Calibrate 12V Voltage Display Value	2	ActualValue*512 12V:00 18
0x18	Calibrate 12VSB Voltage Display Value	2	ActualValue*512 12V:00 18
0x19	Calibrate 12V Current Display Value	2	Actualvalue*4 65A:04 01
0x1E	Clear Black Box Data	2	0xAB 0xCD
0x1F	Calibrate Primary parameters	6	Vin*10/Pin* 10/Iin*1000 230V/600W/2.78A 0xFC 0x08 0x70 0x17 0xDC 0x0A

18 MFR_SPEC Command Details

18.1 Manufacturer Ratings

The commands provide the ability for manufacturers to provide summary information about the unit'sratings. This is a read of the unit's maximum or minimum value with respect to input type.

Example: High/Low Line MFR_IIN_MAX is 18A/9A.

CMD	Name	Input type	Report Value
A0h	MFR_VIN_MIN	High / Low Line,	same
A1h	MFR_VIN_MAX		same
A2h	MFR_IIN_MAX		different
A3h	MFR_PIN_MAX[1]		different
A4h	MFR_VOUT_MIN		same
A5h	MFR_VOUT_MAX		same
A6h	MFR_IOUT_MAX[1]		different
A7h	MFR_POUT_MAX[1]		different
A8h	MFR_TAMBIENT_MAX		same
A9h	MFR_TAMBIENT_MIN		same

Table 42:Manufacturer Ratings

Note:

1. If support High/Low Line with different of max load
2. If support

18.2 Cold Redundancy

18.2.1 Powering on Cold Standby supplies to maintain best efficiency

Power supplies in Cold Standby stateshall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at.

	Enable Threshold for $V_{CR\_ON\_EN}$	Disable Threshold for $V_{CR\_ON\_DIS}$	CR_BUS#
Standard Redundancy(00h) (default power on state)	power supply is always ON		Open

Cold Redundant Active (01h)	power supply is always ON		High(CR signal will be high after PG assert)
Cold Standby 1 (02h)	3.2V (40% of max)	3.2V x 0.5 x 0.9 = 1.44V	Open
Cold Standby 2 (03h)	5.0V (62% of max)	5.0V x 0.5 x 0.9 = 2.25V	Open
Cold Standby 3 (04h)	6.7V (84% of max)	6.7V x 0.5 x 0.9 = 3.015V	Open
Always Standby (05h)	7.8V(97.5% of max)	7.8V x 0.5 x 0.9 = 3.51V	Open

Table 43:Example Current Share Threshold

Notes:

Maximum load share voltage = 8.0V (refer HW SPEC) at 100% of rated output power

These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

CR_BUS#	PSU 1 State	PSU 2 State
Low	Standard Redundancy	Standard Redundancy
High	Cold Redundant Active	Always Standby
High	Cold Redundant Active	Cold Standby
High	Cold Redundant Active	Cold Redundant Active

Table 44:Logic Matrix for Cold Redundancy

18.2.2 Powering on Cold Standby supplies during a fault or over current condition

When an active power supply asserts its CR_BUS# signal (pulling it low), all parallel power supplies in cold standby modeshall power on within 100 µsec.

18.2.3 Cold_Redundancy_Config (D0h)

The MFR command Active Standby (D0h) is used to configure the operating state of the power supply related to cold redundancy.

The power supplies setup to be the cold standby power supplies; shall change to standard redundancy mode (D0h = 00h) whenever the CR_BUS# is pulled low.

D0h	Active Standby	
Value	**State**	**Description**
00h	Standard Redundancy(00h) (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signalshall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active [1]	Defines this power supply to be the one that is always ON in a cold redundancy configuration.

02h	Cold Standby 1 [1]	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2 [1]	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3 [1]	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
05h- FFh	Reserved	

Table 45:Cold_Redundancy_Config

Note: 1. When the CR_BUS# transitions from a high to a low state; each PSU programmed to be in Slave stateshall be put into Standard Redundancy mode (Cold_redundancy_Config = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the Cold_Redundancy_Config command. When an active power supply experience any warning or fault condition, it shall assert its CR_BUS# signal (pulling it low) immediately to assure that all parallel power supplies in cold redundant or active standby mode can power on.

18.3FW_REVISION (D2h)

D0h	FW_Revision		
Byte	Value	Description	Note
0	0x14	Block count	Hex
1	V		ASCII
2	0~9	Secondary major revision	ASCII
3	.		ASCII
4	0~9	Secondary minor revision	ASCII
5	.		ASCII
6	0~9	Secondary minor revision	ASCII
7~20	0x00	Free bytes fill with 0x00	Hex

Table 46:FW_Revision

18.4Black Box Data Recorder

The PSU have the capability to capture and retriever a snapshot of the supply stage once a STATUS register fault indication has occurred excluding SBY_Fault and Vin_UV_Fault. The PSU shutdown fault capture data is to be stored within the “blackbox” of the PSU as a segment of non-volatile memory that can be accessed long afterwards. It should be organized as a 5-deep shift register.

18.4.1 MFR_BLACKBOX_PAGE (E4h)

Any fault that is defined as a blackbox event causes a complete storage of the last known state ofthe supply, not just the fault related variables. (Note that this does not apply to warning or statusconditions). The history is stored at the time of the fault. For example, if an over-temp fault has happened,then reading the temperature returns that last known temperature at the time of the OT fault. Alsoreading Vout (MFR_PAGE = 1) returns the last known output voltage when the OT fault occurred. The datawithin Fault History 1 will be identical to the Real Time Data at the instant the fault occurred. After that time,the Real Time data values will likely diverge since they are not latched. The PSU manufacturershall clearthis fault history prior to the unit'sshipment.

E4h	MFR_PAGE
Value	Description
0xFF	Real Time Data(Default)
0x00	FaultHistory1(newestfaultevent)
0x01	FaultHistory2
0x02	FaultHistory3
0x03	FaultHistory4
0x04	FaultHistory5
other	Reserved, assertinvaliddataflagintheSTAT_CML

Table 47:MFR_PAGE

When the MFR_PAGE is set to 0xFF, any PMBus commands will operate normally (in realtime). When the MFR_PAGE command is used to set the page to 0x00 to 0x04, any following PMBus commands will refer to the value of that parameter stored at the time of the respective fault condition.

Command	Command Name	Command	Command Name
7Ah	STATUS_VOUT	8Eh	READ_TEMPERATURE_2
7Bh	STATUS_IOUT	8Fh	READ_TEMPERATURE_3
7Ch	STATUS_INPUT	90h	READ_FAN_SPEED_1
7Dh	STATUS_TEMPERATURE	96h	READ_POUT
7Eh	STATUS_CML	97h	READ_PIN

81h	STATUS_FAN_1_2	E5h	POS_TOTAL
88h	READ_VIN	E6h	POS_LAST
89h	READ_IIN		
8Bh	READ_VOUT		
8Ch	READ_IOUT		
8Dh	READ_TEMPERATURE_1		

Table 48:Fault History Command

18.5POS_TOTAL (E5h)

This is a read of the Total Power On Seconds (POS) the PSU has been powered on and delivering energy to the main output since it was manufactured. The register must increment in seconds while the main output is delivering energy. When the main output is not delivering energy the PSU must hold the current value. Time accuracy must be within ±5%

18.6POS_LAST (E6h)

This is a read of the Last Power On Seconds (POS) since the PSU has been powered on and delivering energy to the main output since it was last started. This value must be reset to zero when the main output of the PSU is started. The register must increment in seconds while the main output is delivering energy. When the main output is not delivering energy the PSU must hold the current value. Time accuracy must be within ±5%.

18.7 System on-Line Bootloader

The power supplyshall have the capability to update its firmware via the PMBus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the Vst by pins.